

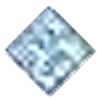


SeeYA 1.03" Micro-OLED (2560×2560RGB)

Specification

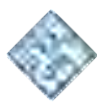
Model Name: SY103WAM01

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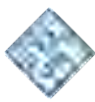
Revision

Version	Date	Description
V1.0	2021.4.15	Initial release



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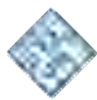


1 General Description

This display is a 1.03 inch diagonal, 2560(RGB) × 2560 dots active matrix color OLED panel module based on single-crystal silicon transistors. This panel integrates panel driver and logic driver, and realizes small size, light weight, low power consumption and high resolution.

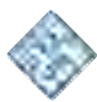
Applications: View finders, Head mounted displays, etc.

- 2560 x 2560 Real RGB Resolution
- AP Operated Resolution
 - 2560 x 2560: (8 x M, M=160~320) x RGB x (8 x N, N=90~320)
- Frame rate:
 - 1920 x1920 input, x1.33scaling up to 2560 x2560, VESA DSC on, maximum 90Hz
 - 2560 x2560, input, x1scaling up , VESA DSC on, maximum 75Hz
- Normal operation supports full color mode: 16.7M colors
- Interface
 - MIPII + I2C
 - MIPI DPHY v1.2 with one / two port (4 / 8 lanes), 1.0Gbps/Lane
 - MIPI DSI v1.01 R11 Video mode
 - Support VESA-DSC v1.1 in-chip decoder (3X compression ratio)
 - Support scaling up 1.33x (1920x1920 to 2560 x 2560) and 2x (1280x1280 to 2560 x 2560)
- Scan direction selection, up or down and right or left
- Orbit supported
- Wide range Brightness adjustment
- Sequential/Global emission
- Temperature compensation



2 General Feature

Parameter	Specification
Resolution	2560(H) x 2560 (V)
Number of dots	19.66M (2560x2560x3)
Pixel Size	7.2μm x 7.2μm
Pixel Arrangement	RGB π type
Useable Display Area	18.432mm x 18.432mm / 1.03" diagonal
Luminance	1800cd/m ² typical
Contrast Ratio	500,000:1 typical
Uniformity	> 85%
Operating Voltage	VDDI=1.8V AVDD=5.8V~6V AVEE=-4V~-5.5V
Power Consumption (1800nits, 100%duty_1920 × 1920input_1.33scaling up_No DSC_72Hz)	1600mW
Gray Levels	256
Interface	MIPI (1 or 2-port D-PHY)
Frame Rate	60HZ~90HZ
Weight	2g
Operating Temperature	-20°C to +70°C
Storage Temperature	-40°C to +80°C



3 Optical Specification

Item	Description	Min.	Typ.	Max.	Unit
Brightness	Tpanel=30°C		1800		cd/m2
Brightness	Tpanel=10°C ~70°C	1350	1800	2250	cd/m2
CR	white to Black Contrast Ratio	200,000:1	500,000:1		
Uniformity	End to end large-area uniformity	85			%
CIE Red	CIE-x	0.635	0.655	0.675	
	CIE-y	0.315	0.335	0.355	
CIE Green	CIE-x	0.197	0.232	0.267	
	CIE-y	0.675	0.695	0.715	
CIE Blue	CIE-x	0.141	0.161	0.181	
	CIE-y	0.045	0.065	0.085	
CIE White	CIE-x	0.298	0.313	0.328	
	CIE-y	0.314	0.329	0.344	
Color Gamut	DCI-P3	80%	90%		
View angle (White)	Luminance decay to 50%	35°			
Frame rate		60		90	HZ
Power consumption	1800nits, 100%duty_1920× 1920input_1.33sca ling up_No DSC_72Hz		1600	2000	mW

Note1: If there is no specified, the specification of optical is specified at 30 degree Celsius.

Note2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. Brightness is measured as peak luminance at full white pattern (Gray level=255);

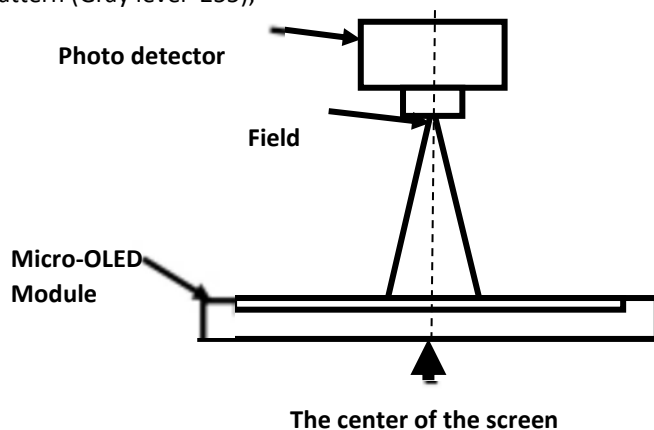
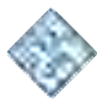


Fig.1



Note3: Definition of Uniformity at highest gray level(255) and 100%duty emission.

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (U)} = L_{\min} / L_{\max}$$

L-----Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

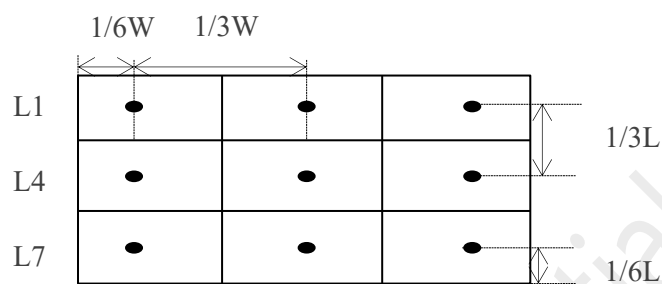
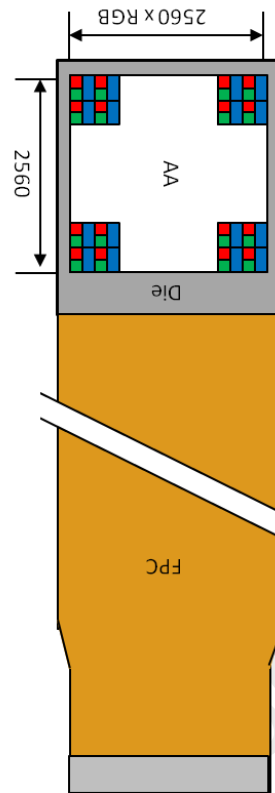
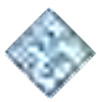


Fig. 2

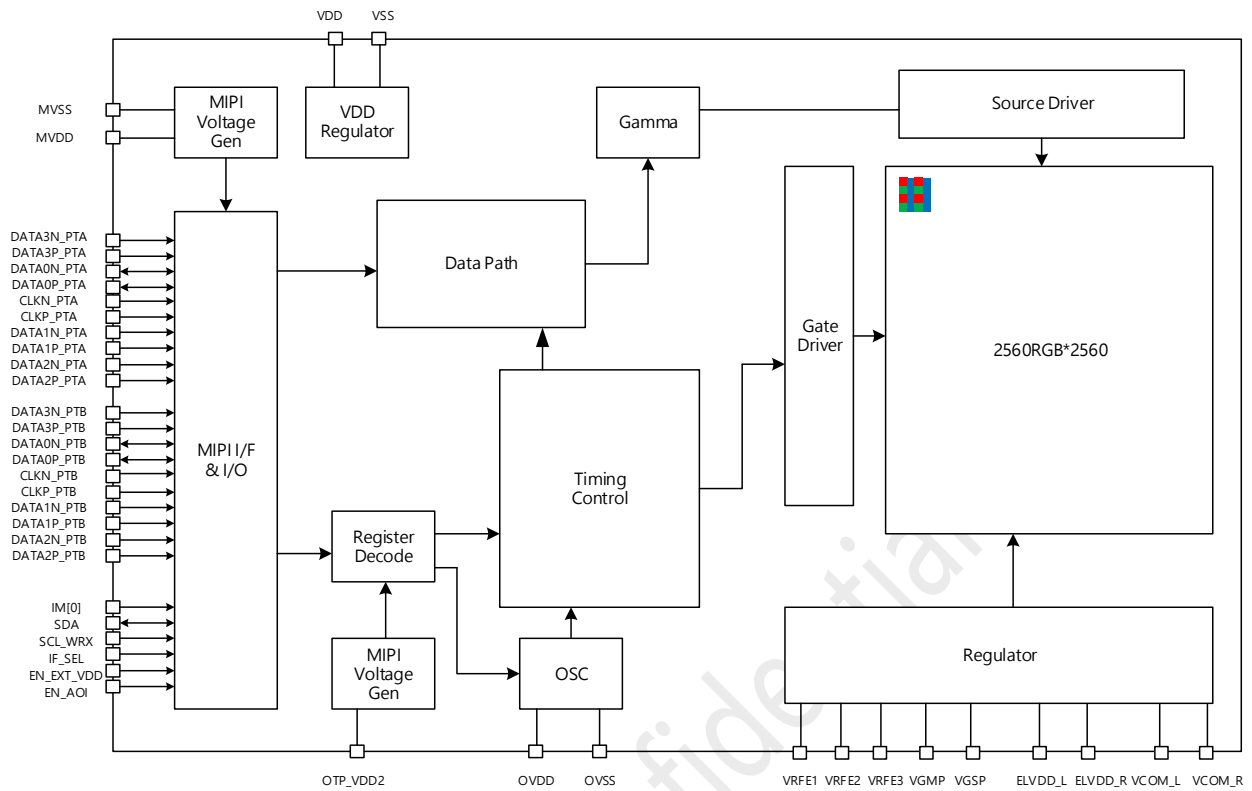


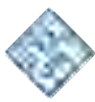
4 Pixel Arrangement



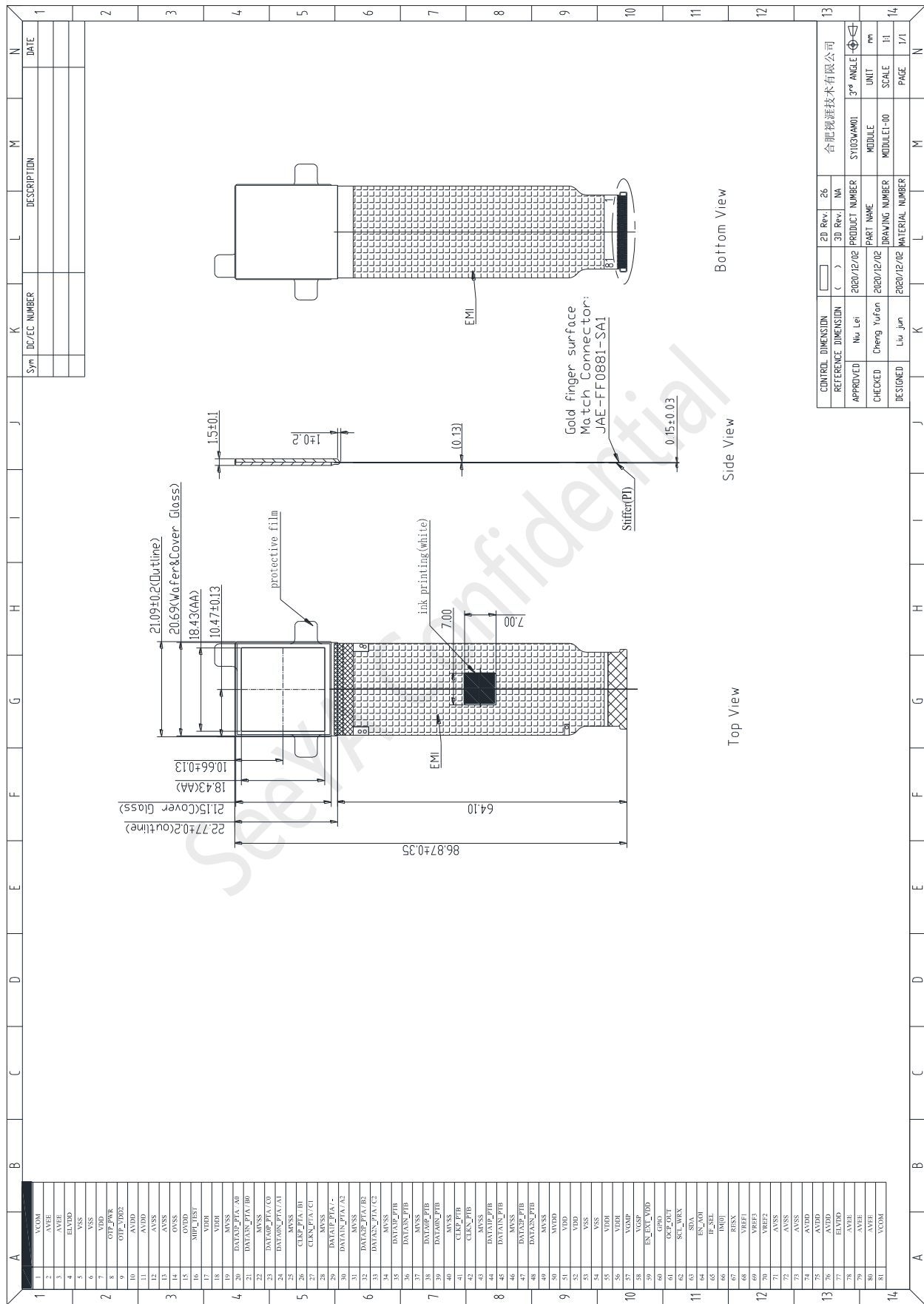


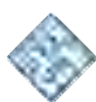
5 System block





6 Module Diagram

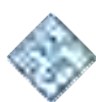




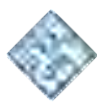
7 Pin Description

7.1 Pin Description

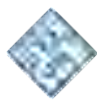
Pin No.	Symbol	Type	Description
1	VCOM	Output	Regulator output for common electrode voltage. connect a capacitor for stabilization, connect a TVS diode to GND.
2	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. connect a capacitor for stabilization.
3	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. then connect a capacitor for stabilization.
4	ELVDD	Output	Power supply for OLED cell. connect a capacitor for stabilization.
5	VSS	Power	System GND for internal digital system.
6	VSS	Power	System GND for internal digital system.
7	VDD	Output	Connect a capacitor for stabilization.
8	OTP_PWR	Input	OTP program power. If not use, please connect to GND or OPEN.
9	OTP_VDD2	Output	Regulator output for MTP analog system power. Connect a capacitor for stabilization.
10	AVDD	Power	5.8V~6.0V Power supply for analog system. connect a capacitor for stabilization.
11	AVDD	Power	5.8V~6.0V Power supply for analog system. connect a capacitor for stabilization.
12	AVSS	Power	System GND for analog system.
13	AVSS	Power	System GND for analog system.
14	OVSS	Power	System GND for oscillator.
15	OVDD	Output	Regulator output for common electrode voltage. Connect a capacitor for stabilization.
16	MIPI_TEST	Input/ Output	Test pin for MIPI.
17	VDDI	Power	Power supply for interface system except for the interface.
18	VDDI	Power	Power supply for interface system except for the interface.
19	MVSS	Power	System GND for MIPI interface.
20	DATA3P_PTA	Input/Output	This pin is DSI D3+ signal if MIPI Port A interface is used. DATA3P/N_PTA is differential small amplitude signals. If not used, please keep it open.
21	DATA3N_PTA	Input/Output	This pin is DSI D3- signal if MIPI Port A interface is used. DATA3P/N_PTA is differential small amplitude signals. If not used, please keep it open.
22	MVSS	Power	System GND for MIPI interface.
23	DATA0P_PTA	Input/Output	This pin is DSI D0+ signal if MIPI Port A interface is used. DATA0P/N_PTA is differential small amplitude signals. If not used, please keep it open.
24	DATA0N_PTA	Input/Output	This pin is DSI D0- signal if MIPI Port A interface is used. DATA0P/N_PTA is differential small amplitude signals. If not used, please keep it open.
25	MVSS	Power	System GND for MIPI interface.
26	CLKP_PTA	Input	This pin is DSI CLK+ signal if MIPI Port A interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
27	CLKN_PTA	Input	This pin is DSI CLK- signal if MIPI Port A interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
28	MVSS	Power	System GND for MIPI interface.
29	DATA1P_PTA	Input/Output	This pin is DSI D1+ signal if MIPI Port A interface is used. DATA1P/N_PTA is differential small amplitude signals. If not used, please keep it open.



30	DATA1N_PTA	Input/Output	This pin is DSI D1- signal if MIPI Port A interface is used. DATA1P/N_PTA is differential small amplitude signals. If not used, please keep it open.
31	MVSS	Power	System GND for MIPI interface.
32	DATA2P_PTA	Input/Output	This pin is DSI D2+ signal if MIPI Port A interface is used. DATA2P/N_PTA is differential small amplitude signals. If not used, please keep it open.
33	DATA2N_PTA	Input/Output	This pin is DSI D2- signal if MIPI Port A interface is used. DATA2P/N_PTA is differential small amplitude signals. If not used, please keep it open.
34	MVSS	Power	System GND for MIPI interface.
35	DATA3P_PTB	Input/Output	This pin is DSI D3+ signal if MIPI Port B interface is used. DATA3P/N_PTB is differential small amplitude signals. If not used, please keep it open.
36	DATA3N_PTB	Input/Output	This pin is DSI D3- signal if MIPI Port B interface is used. DATA3P/N_PTB is differential small amplitude signals. If not used, please keep it open.
37	MVSS	Power	System GND for MIPI interface.
38	DATA0P_PTB	Input/Output	This pin is DSI D0+ signal if MIPI Port B interface is used. DATA0P/N_PTB is differential small amplitude signals. If not used, please keep it open.
39	DATA0N_PTB	Input/Output	This pin is DSI D0- signal if MIPI Port B interface is used. DATA0P/N_PTB is differential small amplitude signals. If not used, please keep it open.
40	MVSS	Power	System GND for MIPI interface.
41	CLKP_PTB	Input	This pin is DSI CLK+ signal if MIPI Port B interface is used. CLKP/N_PTB is differential small amplitude signals. If not used, please keep it open.
42	CLKN_PTB	Input	This pin is DSI CLK- signal if MIPI Port B interface is used. CLKP/N_PTB is differential small amplitude signals. If not used, please keep it open.
43	MVSS	Power	System GND for MIPI interface.
44	DATA1P_PTB	Input/Output	This pin is DSI D1+ signal if MIPI Port B interface is used. DATA1P/N_PTB is differential small amplitude signals. If not used, please keep it open.
45	DATA1N_PTB	Power	This pin is DSI D1- signal if MIPI Port B interface is used. DATA1P/N_PTB is differential small amplitude signals. If not used, please keep it open.
46	MVSS	Input/Output	System GND for MIPI interface.
47	DATA2P_PTB	Input/Output	This pin is DSI D2+ signal if MIPI Port B interface is used. DATA2P/N_PTB is differential small amplitude signals. If not used, please keep it open.
48	DATA2N_PTB	Input/Output	This pin is DSI D2- signal if MIPI Port B interface is used. DATA2P/N_PTB is differential small amplitude signals. If not used, please keep it open.
49	MVSS	Power	System GND for MIPI interface.
50	MVDD	Output	Regulator output for MIPI digital system power. Connect a capacitor for stabilization.
51	VDD	Output	Connect a capacitor for stabilization.
52	VDD	Output	Connect a capacitor for stabilization.
53	VSS	Power	System GND for internal digital system.
54	VSS	Power	System GND for internal digital system.
55	VDDI	Power	power supply for interface system except for MIPI interface.
56	VDDI	Power	power supply for interface system except for MIPI interface.
57	VGMP	Output	Regulator output for gamma high voltage generation. Connect a capacitor for stabilization.
58	VGSP	Output	Regulator output for gamma low voltage generation. Connect a capacitor for stabilization.
59	EN_EXT_VDD	Input	Connect to GND.
60	GPIO	Output	Digital global purpose in/out test pin
61	OCP_OUT	Output	Over current protect output flag.



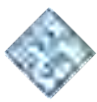
62	SCL_WRX	Input/ Output	Synchronous clock signal in I2C I/F. If this pin is not used, please connect to VDDI.									
63	SDA	Input/ Output	Bi-direction data PIN in I2C I/F. If this pin is not used, please connect to VDDI.									
64	EN_AOI	Input	Connect to GND.									
65	IF_SEL	Input	Connect to GND.									
66	IM[0]	Input	Use to select the Interface type. <table><tr><td>IM[0]</td><td>Command</td><td>Display Data</td></tr><tr><td>0V</td><td>MIPI</td><td>MIPI</td></tr><tr><td>1.8V</td><td>I2C or MIPI</td><td>MIPI</td></tr></table>	IM[0]	Command	Display Data	0V	MIPI	MIPI	1.8V	I2C or MIPI	MIPI
IM[0]	Command	Display Data										
0V	MIPI	MIPI										
1.8V	I2C or MIPI	MIPI										
67	RESX	Input	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.									
68	VREF1	Output	Regulator output for internal reference voltage. Connect a capacitor for stabilization.									
69	VREF3	Output	Regulator output for internal reference voltage. Connect a capacitor for stabilization. Connect a Schottky diode to GND									
70	VREF2	Output	Regulator output for internal reference voltage. Connect a capacitor for stabilization.									
71	AVSS	Power	System GND for analog system.									
72	AVSS	Power	System GND for analog system.									
73	AVSS	Power	System GND for analog system.									
74	AVDD	Power	5.8V~6.0VPower supply for analog system. connect a capacitor for stabilization.									
75	AVDD	Power	5.8V~6.0VPower supply for analog system. connect a capacitor for stabilization.									
76	AVDD	Power	5.8V~6.0VPower supply for analog system. connect a capacitor for stabilization.									
77	ELVDD	Power	Power supply for OLED cell. connect a capacitor for stabilization.									
78	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. connect a capacitor for stabilization.									
79	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. connect a capacitor for stabilization.									
80	AVEE	Power	-4.0V~-6.0V Power supply for OLED cell. connect a capacitor for stabilization.									
81	VCOM	Output	Regulator output for common electrode voltage. connect a capacitor for stabilization, connect a TVS diode to GND.									



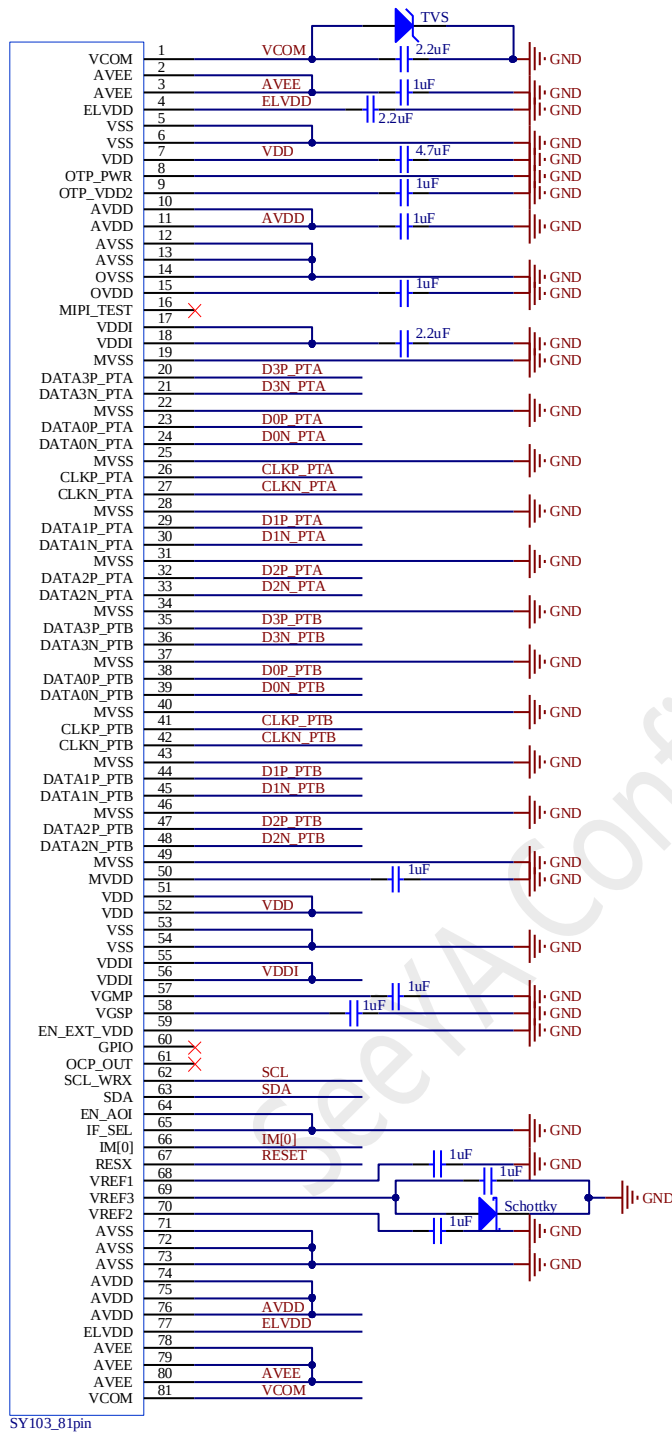
7.2 Application circuit

Below table is the instruction of peripheral circuit. Regarding power supply capacitor connections, mount an appropriate capacitor for each power supply.

No.	Signal Name	Typical Value	Maximum Rated Voltage	Note
1	VDDI	Cap, 2.2uF	6.3V	-
2	AVDD	Cap, 1.0uF	10V	-
3	ELVDD	Cap, 2.2uF	10V	-
4	AVEE	Cap, 1uF	10V	-
5	VDD	Cap, 4.7uF	6.3V	-
6	MVDD	Cap, 1uF	6.3V	-
7	VGMP	Cap, 1uF	10V	-
8	VGSP	Cap, 1uF	10V	-
9	VREF1	Cap, 1uF	6.3V	-
10	VREF2	Cap, 1uF	6.3V	-
11	VREF3	Cap, 1uF Schottky Diode	6.3V	
12	VCOM	Cap, 2.2uF TVS	10V	Recommend: TVS VBR min>8V
13	OTP_VDD2	Cap, 1uF	6.3V	-
14	OVDD	Cap, 1uF	6.3V	-



Below circuit is one of typical example for reference to drive the module with D-PHY.



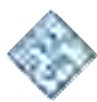
Notes:

I2C Bus: Pin62 SCL and Pin63 SDA.
If I2C is not used, please connect to VDDI.

IM[0]: Use to select the interface type.
(If you connect this pin to GND, only MIPI can execute command. If you connect this pin to VDDI, MIPI or I2C can execute command.)

Schottky: RB521CS30L

TVS: DY2L5A0C0L1



8 Electrical Characteristics

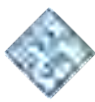
8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When this Micro-OLED product is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use this Micro-OLED product within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this Micro-OLED product will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	5.5	V
Power Supply Voltage (2)	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
Power Supply Voltage in AOI mode	VDDI	1.32	V
	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
MIPI Differential Input	CLKP_PTA/B, CLKN_PTA/B DATAP0_PTA/B, DATAN0_PTA/B DATAP1_PTA/B, DATAN1_PTA/B DATAP2_PTA/B, DATAN2_PTA/B DATAP3_PTA/B, DATAN3_PTA/B	1.32	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI+0.3	V
Operating temperature	Topr	-20 ~ 70	°C
Storage temperature	Tstg	-40 ~ 80	°C

8.2 DC Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage						
AVDD Input Level	AVDD	-	5.8		6.0	V
Digital I/O Power Supply (non-MIPI I/O)	VDDI	-		1.8		V
Digital I/O Input Level @Logic High	VIH	VDDI=1.65V ~ 1.95V	0.7*VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	VIL	VDDI=1.65V ~ 1.95V	0	-	0.3*VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1mA	0.8*VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1mA	0	-	0.2*VDDI	V
Digital I/O Input leakage @Logic High	IIHD	Vin = VDDI			1	uA
Digital I/O Input leakage @Logic Low	IILD	Vin = 0	-1			uA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V
MIPI Input leakage @Logic High	IIHMD	Vin = MVDD			1	uA
MIPI Input leakage @Logic Low	IILMD	Vin = 0	-1			uA



8.3 DSI DC/AC Characteristic

8.3.1 Receiver characteristic

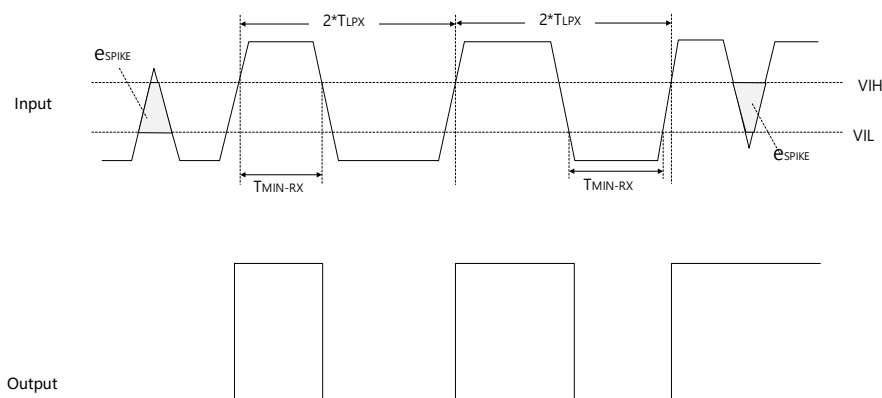
High speed receiver characteristic

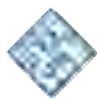
Parameter	Description	Min	Typ.	Max	Unit
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IDTH}	Differential input high threshold	-	-	70	mV
V_{IDTL}	Differential input low threshold	-70	-	-	mV
V_{IHHS}	Single-ended input high voltage	-	-	460	mV
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV
C_{CM}	Common-mode termination	-	-	60	pF



Low power receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
V_{IH}	Logic 1 input voltage	880	-	-	mV
V_{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV
V_{IL_ULPS}	Logic 0 input voltage, ULP state	-	-	300	mV
V_{HYST}	Input hysteresis	25	-	-	mV
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps
T_{MIN-RX}	Minimum pulse width response	20	-	-	





8.3.2 Transmitter Characteristics

High-Speed Transmitter Characteristics

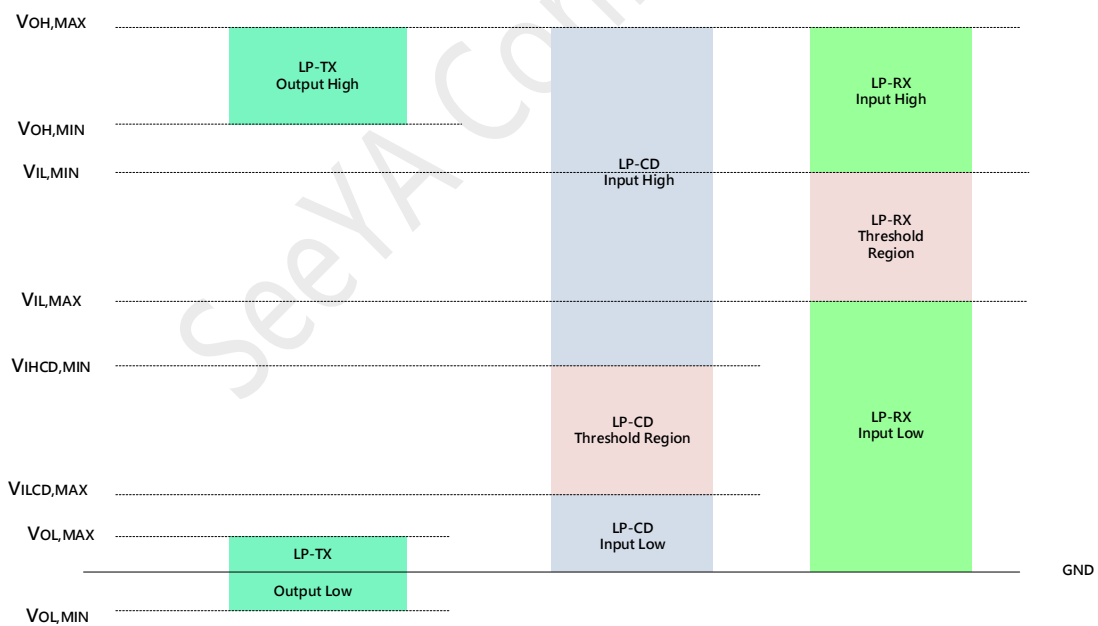
Parameter	Description	Min	Typ.	Max	Unit
V _{CMTX}	HS transmit static common-mode voltage	150	200	250	mV
V _{OD}	HS transmit differential voltage	140	200	270	mV
V _{OHHS}	HS output high voltage	-	-	360	mV
Z _{OS}	Single ended output impedance	40	50	62.5	Ω
t _R and t _F (note1,2)	20%-80%rise time and fall time	-	-	0.3	UI
		-	-	0.35	UI

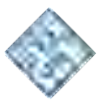
Note:

1. Applicable when supporting maximum HS bitrates ≤ 1Gbps (UI≥1ns)

Low-Power Transmitter Characteristics

Parameter	Description	Min	Typ.	Max	Unit
V _{OH}	The output high level	1.1	1.2	1.3	V
V _{OL}	The output low level	-50	-	50	mV
Z _{OLP}	Output impedance of LP transmitter	110	-	-	Ω
V _{IHCD}	Logic1 contention threshold	450	-	-	mV
V _{ILCD}	Logic0 contention threshold	-	-	200	mV

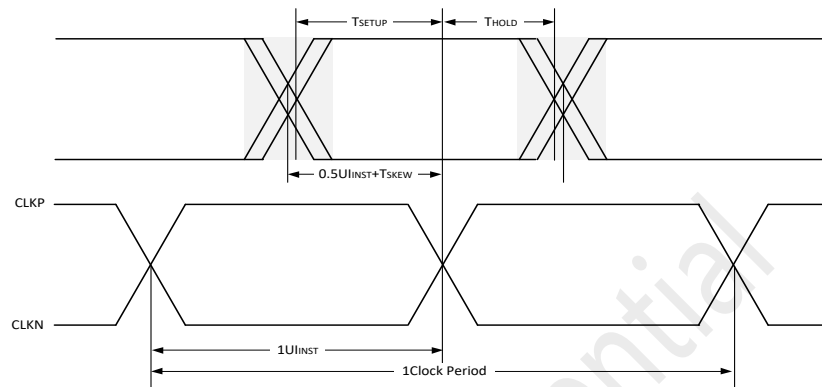


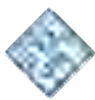


8.4 Timing Characteristics

8.4.1 High Speed Mode Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS

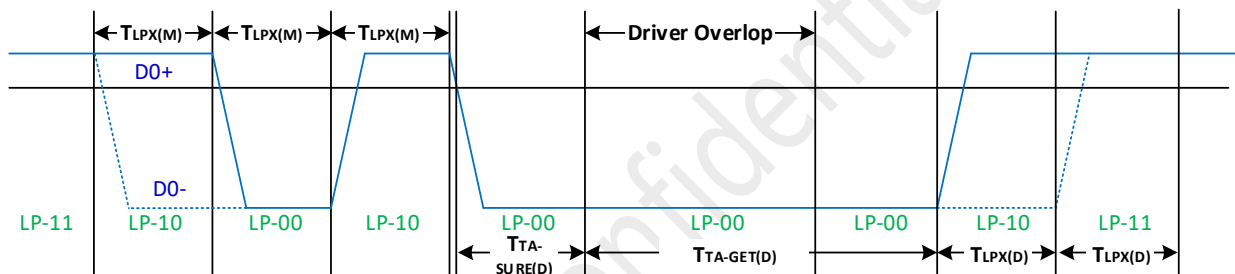




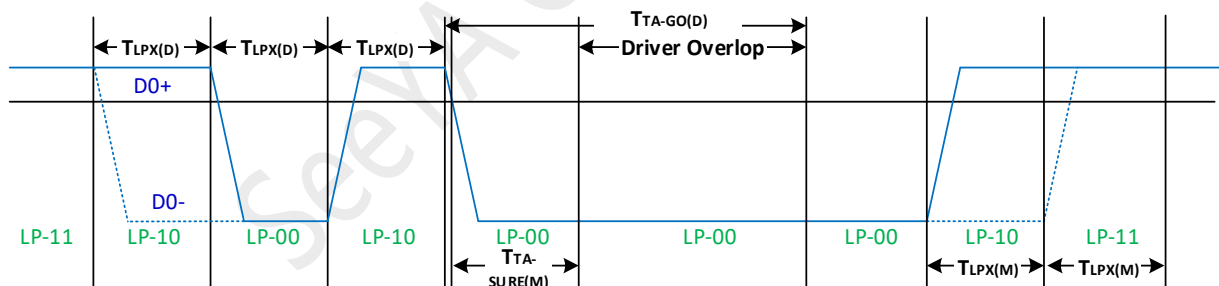
8.4.2 Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state(LP-00) during a Link Turnaround	T_{LPX}	-	$2 * T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround	$5 * T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	$4 * T_{LPX}$			

- Bus Turnaround from MPU to display module

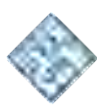


- Bus Turnaround from display module to MPU

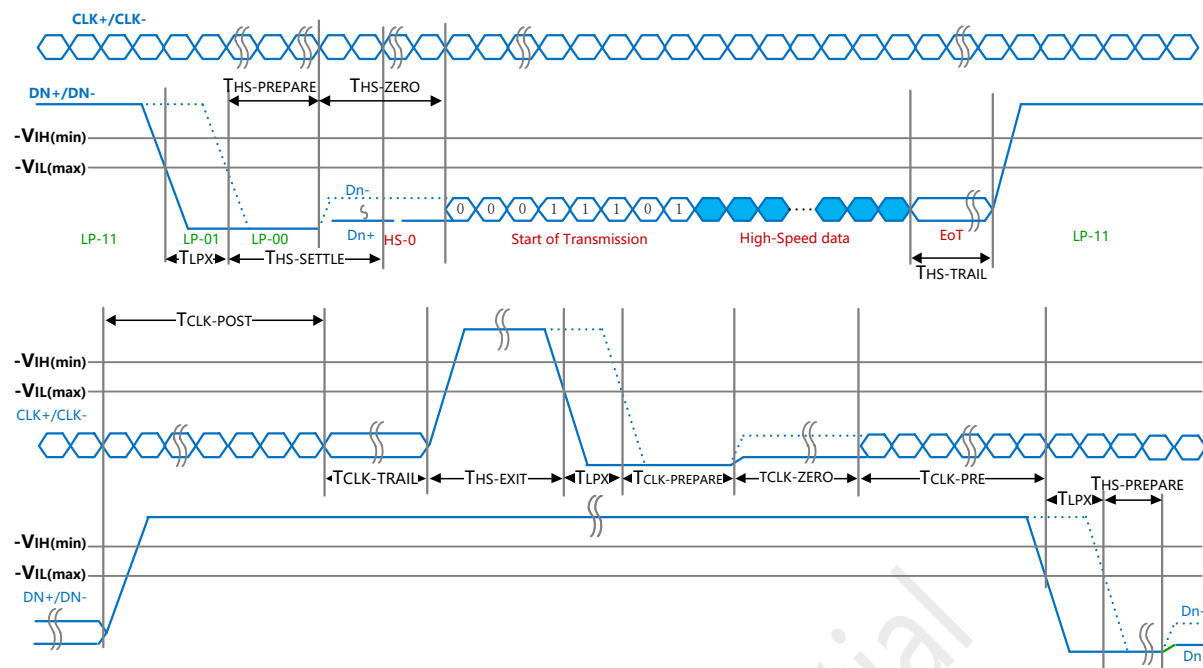
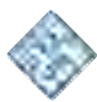


8.4.3 High Speed Mode Operation Timing Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning	$60ns + 52 * U_I$	-	-	ns

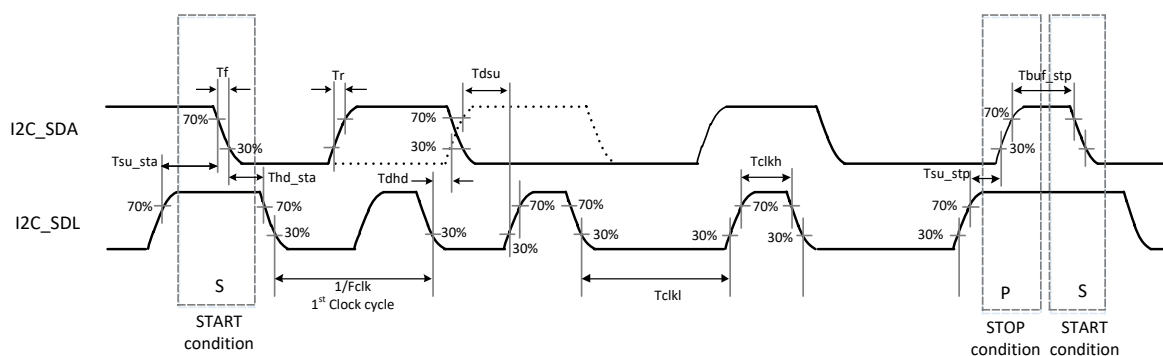


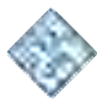
	of TCLK-TRAIL				
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	-	300	ns
$T_{CLK-TERM_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60	-	-	ns
$T_{CLK-PREPARE}+T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
T_{D-TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	35ns+4* UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns+4* UI	-	85ns+6* UI	ns
$T_{HS-PREPARE}+T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns+10*UI	-	-	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns+6* UI	-	145ns+10*UI	ns



8.4.4 I2C-Bus Interface Timing

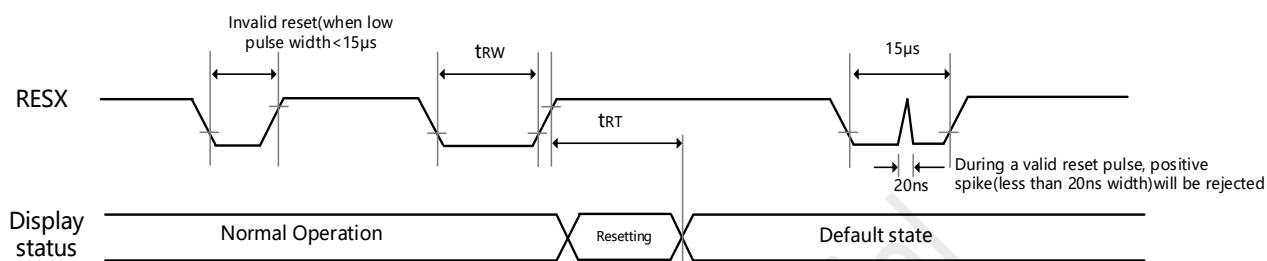
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditio
I2C Clock Frequency	Fclk	-	-	400	kH	
I2C Clock Low	Tckl	130	-	-	ns	
I2C Clock High	Tckh	600	-	-	ns	
I2C Data Rising Time	Tdr	-	-	300	ns	
I2C Data Falling Time	Tdf	-	-	300	ns	
I2C Data Setup Time	Tdsu	100	-	-	ns	
I2C Data Hold Time	Tdhd	-	-	TBD	ns	
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns	
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns	
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns	
I2C Bus Free Time (Stop Condition)	Tbuf_stp	130	-	-	ns	





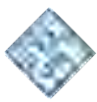
8.5 Reset Timing Characteristics

When Reset happens in Sleep-out mode, this Micro-OLED product will enter blanking sequence with the maximum time 120 msec. Then this Micro-OLED product will remain in blanking state and return \ default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.



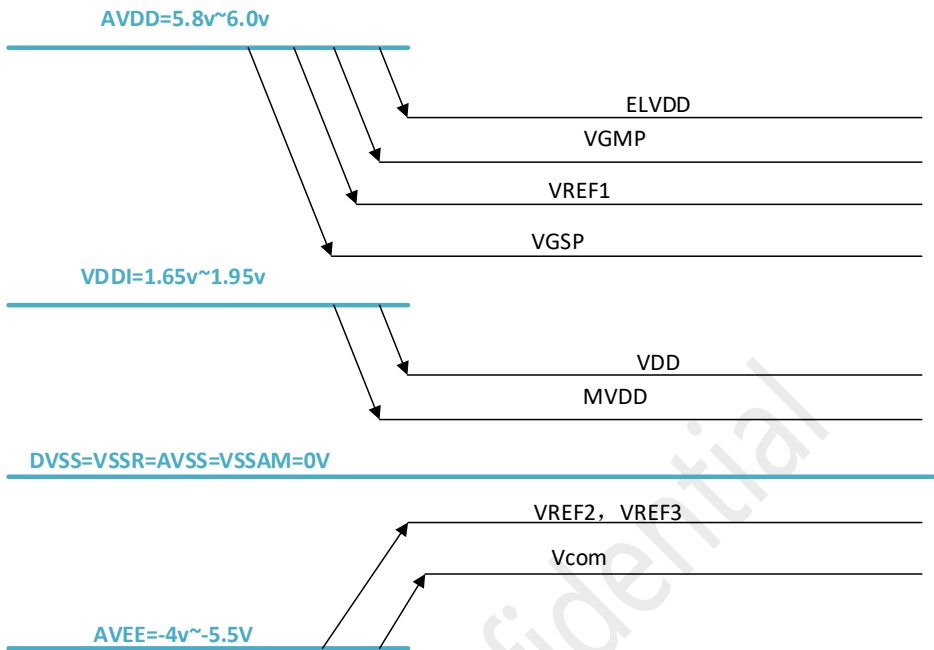
Reset time @VDDI=1.65V to 1.95V, AVSS = VSS = MVSS = 0V, Ta=-40°C to 85°C

Signal	Symbol	Parameter	Min	Typ.	Max	Unit	Description
RESX	tRW	Reset low pulse width	15			us	
	tRT	Reset Complete time			20	ms	When reset applied at sleep-in mode
					120	ms	When reset applied at sleep-out mode



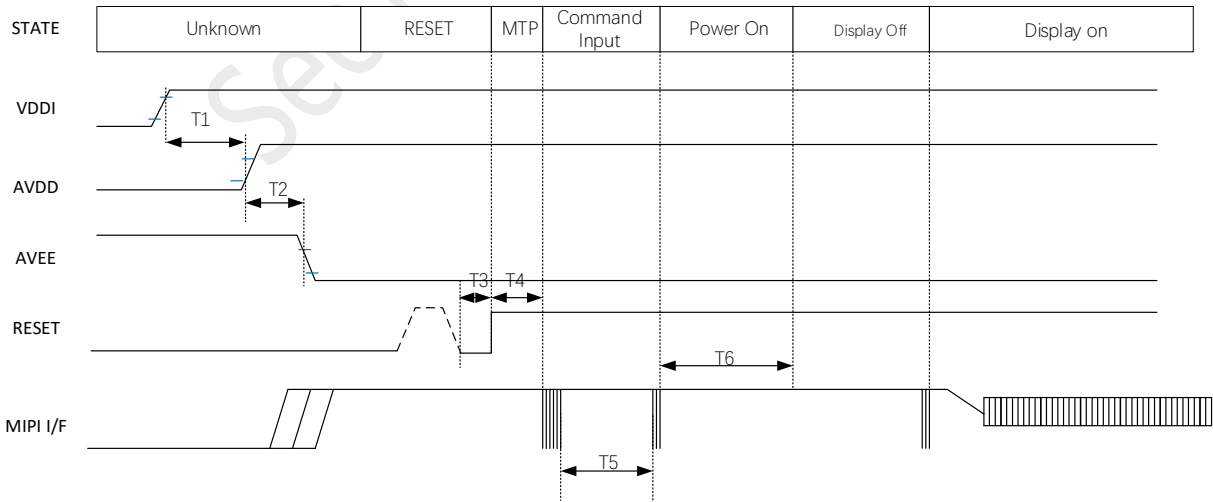
9 Power Sequence

9.1 Power Generation Scheme

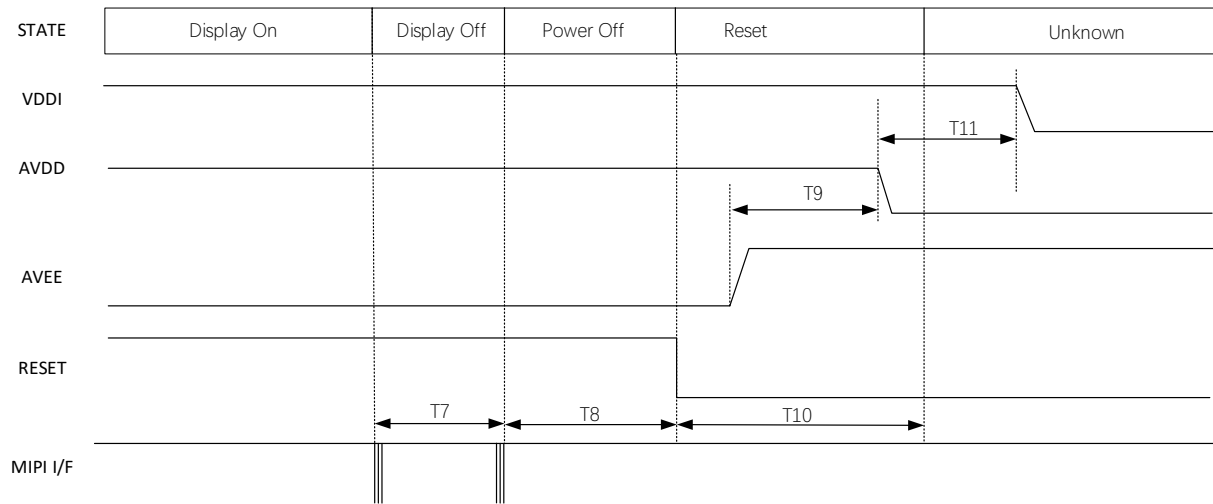
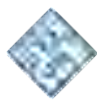


9.2 Power Sequence

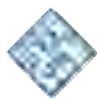
Power on sequence



Power off sequence



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between VDDI and AVDD
T2	2	-	-	ms	Power on time between AVDD and AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	OTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	uS	Power on sequence, the period can be modified
T7	1	-	-	uS	Blanking region
T8	-	1	-	uS	Power off sequence, the period can be modified
T9	2	-	-	ms	Power off time between AVEE and AVDD
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVDD and VDDI

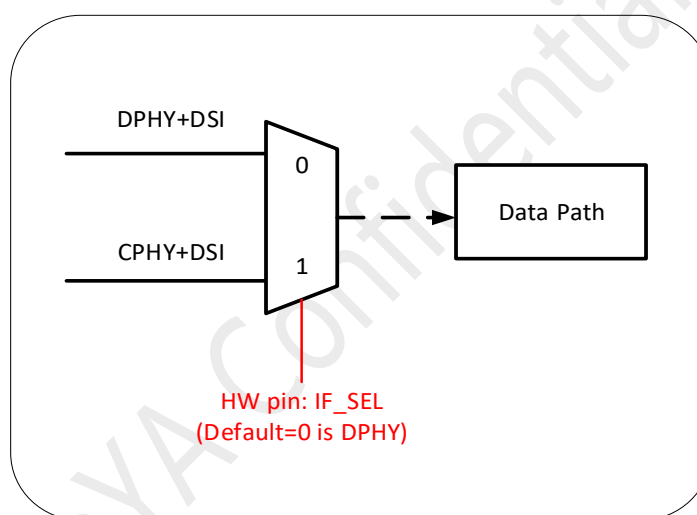


10 Interface

This Micro-OLED product supports MIPI interface and inter-integrated circuit interface (I2C). 1 port MIPI or 2 port MIPI is selected by register, and I2C is selected by IM0, the detail interface selection by IM0 pin and register of PORT1_2_SEL shows in below table.

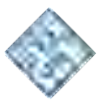
IM0	PORT1_2_SEL	Command Execute	Image Write
0	0	MIPI	MIPI 1port
0	1	MIPI	MIPI 2 port
1	0	I2C or MIPI	MIPI 1port
1	1	I2C or MIPI	MIPI 2 port

This Micro-OLED product supports MIPI interface with D-PHY and C-PHY which is selected by IF_SEL pin.



10.1 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte maybe sent. The master generates all clock pulses, including the ninth acknowledge clock pulse.

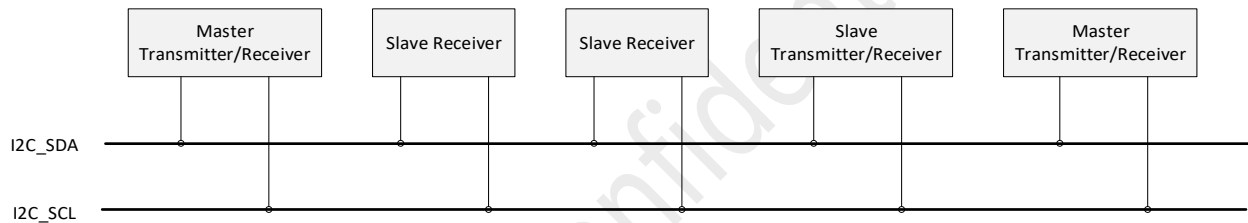


10.1.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition

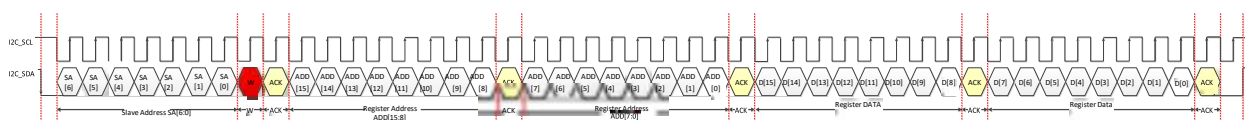
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



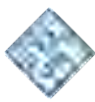
10.1.2 Write Sequence

This Micro-OLED product supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

- (1) Data transfer for register writing should follow the format shown as below.
- (2) After the START condition, a slave address is sent. R/W bit is setting to "0" for Write.
- (3) The slave issues an ACK to the master.
- (4) 8-bits register address transfer first then transfer the register data parameter.
- (5) A data transfer is always terminated by a STOP condition.
- (6) The chip SA [6:0] = 1001100.

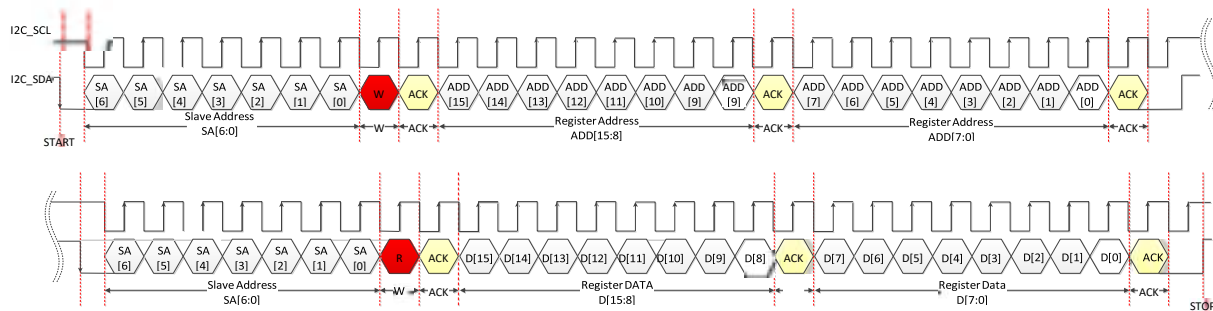


W: Write Bit, W= "1" here, R: Read Bit, R= "0" here
ACK: Acknowledge Bit, ACK= "0" here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data



10.1.3 Read Sequence

This Micro-OLED product supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W: Write Bit, W= "0" here, R: Read Bit, R= "1" here
ACK: Acknowledge Bit, ACK= "0" here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data
NACK: Negative Acknowledge Bit, NACK= "1" here

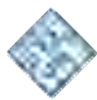
10.2 MIPI Interface

Display serial interface (DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set. The detail Lane configuration for DPHY and CPHY are listed below.

[DPHY]

For DPHY, there are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and this Micro-OLED product shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

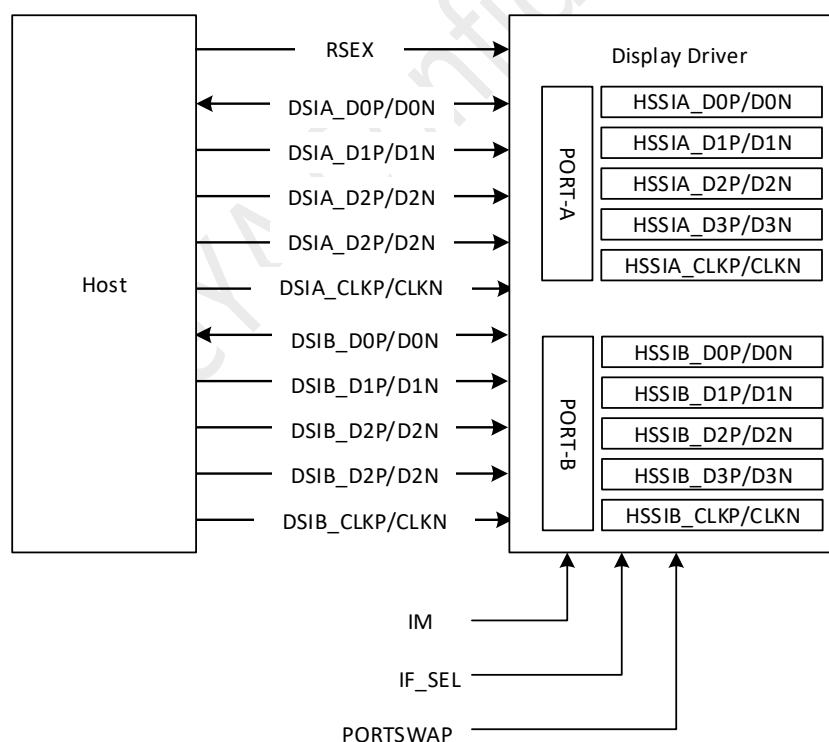
**[DPHY]**

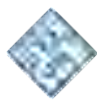
For CPHY, there is no Clock Lane since it's embedded clock in Data Lane. There are 1~3 Trio (Lane) in CPHY. The configuration for CPHY between host and this Micro-OLED product shows as the table below.

Trio	Available Operation Mode	
Trio 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Trio 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Trio 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

10.2.1 DSI System Configuration**[DPHY]**

This Micro-OLED product supports MIPI 2 port with 2, 3 or 4 lane configurations for DPHY. The system configuration is shown as the figure below. There are HW pin(IM, IF_SEL, PORTSWAP) and registers (Lane_num_cfg, PSWAP, DSWAP) which can set the interface and lane related configuration.

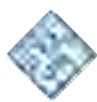




11 User Command

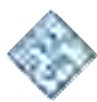
Command list

Instruction	R/W	Address		D7	D6	D5	D4	D3	D2	D1	D0	Default
		MIPI	Non-MIPI									
SWRESET	W	01h	0100h	No Parameter								N/A
CMODE	R/W	03h	0300h	slice2_sel	-	-	-	-	-	-	CMODE	80h
SLPIN	W	10h	1000h	No Parameter								N/A
SLPOUT	W	11h	1100h	No Parameter								N/A
ALLPOFF	W	22h	2200h	No Parameter								N/A
ALLPON	W	23h	2300h	No Parameter								N/A
TCON	R/W	25h	2500h	-	-	-	-	-	-	-	TC_ENABLE	00h
DSPOFF	W	28h	2800h	No Parameter								N/A
DSPON	W	29h	2900h	No Parameter								N/A
CASET	R/W	2Ah	2A00h	XS[15:8]								00h
	R/W		2A01h	XS[7:0]								00h
RASET	R/W	2Bh	2B00h	YS[15:8]								00h
	R/W		2B01h	YS[7:0]								00h
TEON	R/W	35h	3500h	-	-	-	-	-	-	-	M	00h
MADCTL	R/W	36h	3600h	-	-	-	-	RGB	-	RSMX	RSMY	00h
IDMOFF	R/W	38h	3800h	No Parameter								N/A
IDMON	R/W	39h	3900h	No Parameter								N/A
SCACTRL	W	69h	6900h							SC_MOD_SEL[1:0]		00h
IFCONFIG	R/W	6Bh	6B00h	-	-	-	PORT1_2_SEL_CMD1	-	-	-	-	10h
RESCTRL1	R/W	80h	8000h	-	-	-	-	-	-	-	OSC_FREQ_SEL	01h
			8001h	NC[7:0]								40h
			8002h	NL[7:0]								40h
			8003h	-	-	-	NC[8]	-	-	-	NL[8]	11h



SWRESET(0100h): Software Reset

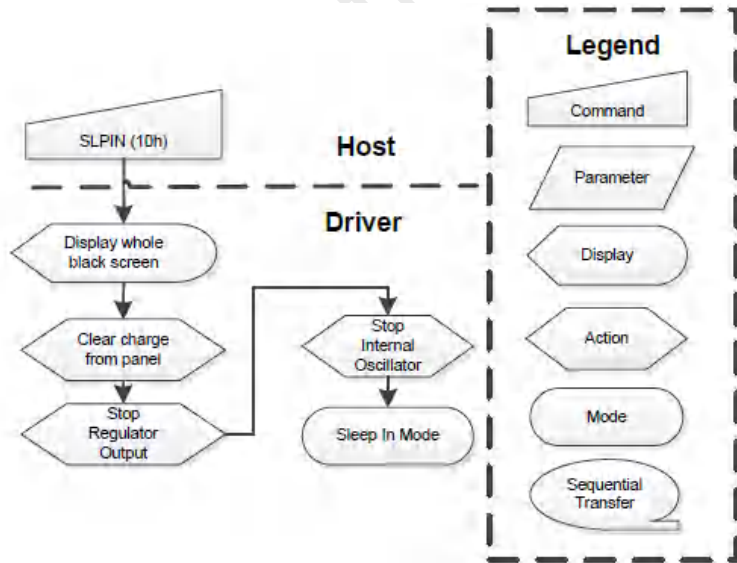
0100H				SWRESET									
Instruction	R/W	Address		Parameter									
		MI	Oth	D ₁	D7	D6	D5	D4	D3	D2	D1	D0	
SWRESET	W	01	0100	-	No Parameter								
Description	When the Software Reset command is executed, all related register and parameters are reset to their S/W Reset default values.												
Restriction	It is necessary to wait 10m sec to send any command following the S/W Reset. If S/W Reset is executed in Sleep-out mode, it is necessary to wait 120m sec to send Sleep-Out command. The Software Reset command cannot be sent during Sleep-Out sequence. Any new command cannot be sent within 8-frame until device enters Sleep-In mode.												
Default	Status			Default Value									
	Power On Sequence			0100h					N/A				
	SW Reset			The same as above									
	HW Reset			The same as above									
Flow Chart	SWRESET (01h) ↓ Display blank screen ↓ Set commands to S/W default value ↓ Sleep-In Mode Host Driver Legend Command Parameter Display Action Mode Sequential Transfer												



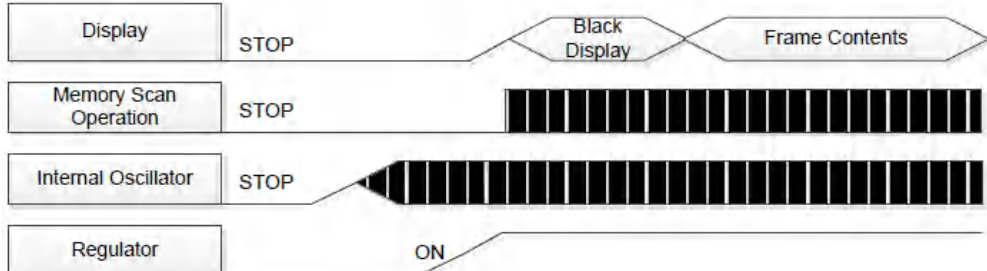
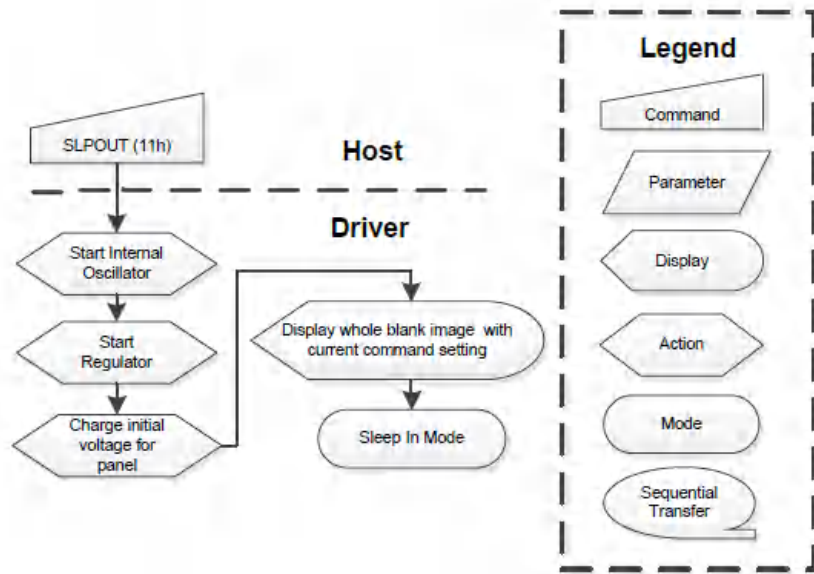
CMODE(0300h): Compression Mode

0400H		RDID123										
Instruction n	R/W	Address		Parameter								
		MI 03h	Oth 0300h	D 1	D7	D6	D5	D4	D3	D2	D1	D0
CMODE	R/W	03h	0300h	-	D7							D0
Description n	These commands are used for compression mode											
	Bit		Symbol		Description						Comment	
	D7		slice_sel		Compression slice selection						0=1 slice 1=2 slice	
	D0		CMODE		Enable/Disable compression mode						0=Disable 1=Enable	
Restriction	-											
Default	Status		Default Value									
	Power On Sequence		0300h					80h				
	SW Reset		The same as above									
	HW Reset		The same as above									
Flow Chart	CMODE (03h) ↓ CMODE Slice_sel ↓ New Compression mode Host Driver Legend Command Parameter Display Action Mode Sequential Transfer											

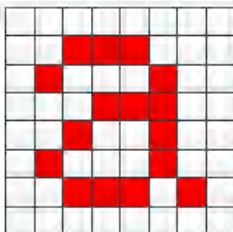
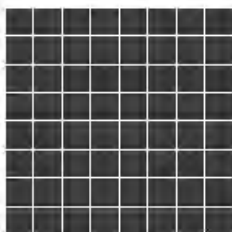
SLPIN (1000h): Sleep In

1000H	SLPIN											
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	W	10	1000	-	No Parameter							
Description	This command force display module to enter <i>Sleep-In</i> mode. Under <i>Sleep-In</i> mode, internal display oscillator, and panel scanning are all stopped. The interface and related registers are still working and keeps its values.											
												
Restriction	-											
Default	Status		Default Value									
	Power On Sequence		1000h					Sleep In Mode				
	SW Reset		The same as above									
	HW Reset		The same as above									
Flow Chart												

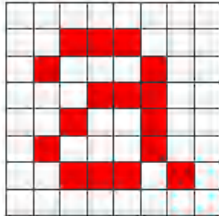
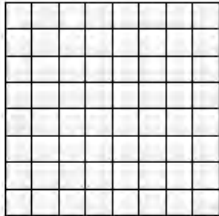
SLPOUT (1100h): Sleep Out

1100H		SLPOUT											
Instruction	R/W	Address		Parameter									
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0	
SLPOUT	W	11	1100	-	No Parameter								
Description	This command force display module to exit <i>Sleep-In</i> mode. Under <i>Sleep-out</i> mode regulator, internal display oscillator, and panel scanning are all enabled.												
													
Restriction	-												
Default	Status		Default Value										
	Power On Sequence		1100h				Sleep In Mode						
	SW Reset		The same as above										
	HW Reset		The same as above										
Flow chart													

ALLPOFF (2200h): All Pixels OFF

2200H	ALLPOFF											
Instruction	R/W	Address		Parameter								
		MI	Othe	D ₁	D7	D6	D5	D4	D3	D2	D1	D0
ALLPOFF	W	22	2200	-	No Parameter							
Description	This command forces the display module to display black image in <i>Display-On Mode</i> .											
	Input Image  → Display 											
Restriction	-											
Default	Status			Default Value								
	Power On Sequence			2200h					All Pixel Off			
	SW Reset			The same as above								
	HW Reset			The same as above								
Flow Chart	Normal Display On mode ↓ ALLPOFF(22h) ↓ Display Black Image Legend Command Parameter Display Action Mode Sequential Transfer											

ALLPON (2300h): All Pixel ON

2300H		ALLPON											
Instruction	R/W	Address		Parameter									
		MI	Othe	D ₁	D7	D6	D5	D4	D3	D2	D1	D0	
ALLPON	W	23	2300	-	No Parameter								
Description	This command forces the display module to display white image in <i>Display-OnMode</i> .												
	Input Image  → Display 												
Restriction	-												
Default	Status			Default Value									
	Power On Sequence			2300h					All Pixel Off				
	SW Reset			The same as above									
	HW Reset			The same as above									
Flow Chart	Normal Display On mode ↓ ALLPON(23h) ↓ Display White Image Legend Command Parameter Display Action Mode Sequential Transfer												

TCON (2500h): Temperature Sensor Enable

2300H				ALLPON								
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
ALLPON	R/W	25	2500	-	-	-	-	-	-	-	-	D0
Description	This command is used to turn on temperature sensor.											
	Bit	Symbol	Description							Comment		
	D0	TC_ENABLE	Temperature sensor enable							0=Temperature sensor off 1=Temperature sensor on		
Restriction												
-												
Default	Status		Default Value									
	Power On Sequence		2500h						00h			
	SW Reset		The same as above									
	HW Reset		The same as above									
Flow Chart	TCON(25h) Parameter TC_ENABLE Temperature Sensor On Host Driver Legend Command Parameter Display Action Mode Sequential Transfer											

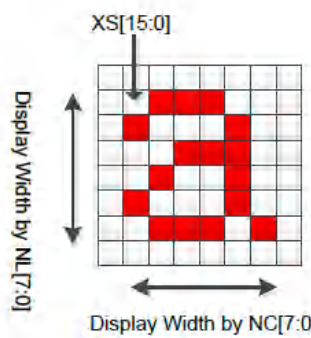
DISPOFF (2800h): Display OFF

2800H				DISPOFF									
Instruction	R/W	Address		Parameter									
		MI	Other	D ₁	D7	D6	D5	D4	D3	D2	D1	D0	
DISPOFF	W	28	2800	-	No Parameter								
Description	This command forces the display module to stop displaying imagedata.												
Restriction	This command has no effect when display driver is already in <i>DISPLAY-OFF</i> mode												
Default	Status			Default Value									
	Power On Sequence			2800h					Display Off				
	SW Reset			The same as above									
	HW Reset			The same as above									
Flow Chart	Display ON mode ↓ DISPOFF(28h) ↓ Display OFF mode Legend Command Parameter Display Action Mode Sequential Transfer												

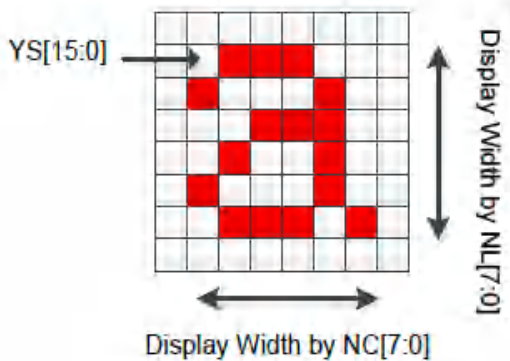
DISPON (2900h): Display ON

2900H	DISPON											
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	W	29	2900	-	No Parameter							
Description	This command forces the display module to start displaying image data.											
Restriction	This command has no effect when display driver is already in <i>DISPLAY-ON</i> mode.											
Default	Status		Default Value									
	Power On Sequence		2900h					Display Off				
	SW Reset		The same as above									
	HW Reset		The same as above									
	Display OFF mode ↓ DISPON(29h) ↓ Display ON mode Legend Command Parameter Display Action Mode Sequential Transfer											

CASET (2A00h): Column Address Set

2A00H	CASET											
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
CASET	R/W	2A0h	2A00	-	XS[15:8]							
			2A01	-	XS[7:0]							
Description	This command indicates display start position of display module in columns. XS[15:0]: Display line start position. 											
Restriction	1. XS= 0 + 2N, N=integer 2. Display content can be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. XS should follow the rule as below: PIXEL_SHIFT_X_DIR=0(Left) Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 - PIXEL_SHIFT_X_COUNT*2 ≤ 2568 (A08h) PIXEL_SHIFT_X_DIR=1(Right) Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 + PIXEL_SHIFT_X_COUNT*2 ≤ 2568 (A08h)											
Default	Status			Default Value								
	Power On Sequence	2A00h				00h						
		2A01h				00h						
	SW Reset	The same as above										
	HW Reset	The same as above										

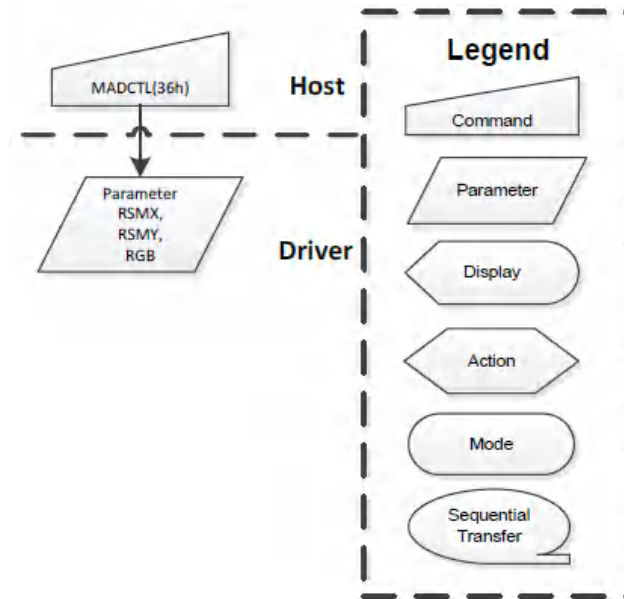
RASET (2B00h): Row Address Set

2A00H			CASET										
Instruction	R/W	Address		Parameter									
		MI	Othe	D ₁	D7	D6	D5	D4	D3	D2	D1	D0	
RASET	R/W	2Bh	2B00	-	YS[15:8]								
			2B01	-	YS[7:0]								
Description	This command indicates display start position of display module in rows. XS[15:0]: Display line start position. 												
Restriction	1. YS= 0 + 2N, N=integer 2. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. YS should follow the rule as below: PIXEL_SHIFT_Y_DIR=0(Up) Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 - PIXEL_SHIFT_Y_COUNT*2 ≤ 2568 (A08h) PIXEL_SHIFT_Y_DIR=1(Down) Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 + PIXEL_SHIFT_Y_COUNT*2 ≤ 2568 (A08h)												
Default	Status			Default Value									
	Power On Sequence			2B00h					00h				
				2B01h					00h				
	SW Reset			The same as above									
HW Reset			The same as above										
Display in Idle mode RASET (2Bh) Display Area adjusted by YS setting Legend Command Parameter Display Action Mode Sequential Transfer													

MADCTL (3600h): Set Address Mode

3600H		MADCTL																									
Instruction	R/W	Address		Parameter																							
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0															
MADCTL	R/W	36	3600	-	-	-	-	-	D3	-	D1	D0															
Description	This command set scan direction of source and gate and data order.																										
	Bit		Symbol		Description				Comment																		
	D3]		RGB		Color Order of sub-pixel of true RGB type				1=BGR 0=RGB																		
	D1		RSMX		Horizontal Flip				1=Normal Display 0= Horizontal Flip																		
	D0		RSMY		Vertical Flip				1= Normal Display 0= Vertical Flip																		
	Input image <table><tr><th>RSMX</th><th>RSMY</th><th>Display</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table>												RSMX	RSMY	Display	0	0		0	1		1	0		1	1	
	RSMX	RSMY	Display																								
	0	0																									
	0	1																									
	1	0																									
1	1																										
Input Data order <table><tr><th>RGB</th><th>Panel Display Color Order</th></tr><tr><td>0</td><td></td></tr><tr><td>1</td><td></td></tr></table>												RGB	Panel Display Color Order	0		1											
RGB	Panel Display Color Order																										
0																											
1																											
Restrictio	-																										
Default	Status		Default Value																								
	Power On Sequence		3600h					00h																			
	SW Reset		The same as above																								
	HW Reset		The same as above																								

Flow Chart



IDMOFF (3800h): Idle Mode Off

3800H	IDMOFF												
Instruction	R/W	Address		Parameter									
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0	
IDMOFF	W	38	3800	-	No Parameter								
Description	This command cause display module to exit <i>Idle</i> mode.												
Restriction	This command has no effect when display module is not in <i>Idle</i> mode.												
Default	Status			Default Value									
	Power On Sequence			3800h					Idle mode off				
	SW Reset			The same as above									
	HW Reset			The same as above									
Flow Chart	Idle mode On ↕ IDMOFF(38h) ↕ Idle mode Off Host Driver Host Legend Command Parameter Display Action Mode Sequential Transfer												

IDMON (3900h): Idle Mode On

3900H		IDMON											
Instruction n	R/W	Address		Parameter									
		MI 39	Othe 3900	D 1 -	D7	D6	D5	D4	D3	D2	D1	D0	
IDMON	W	39	3900	-	No Parameter								
Description	This command cause display module to enter <i>Idle</i> mode. In the <i>idle</i> mode, color expression is reduced.												
	Input Image → Display												
Restriction	This command has no effect when display module is already in <i>Idle</i> mode.												
Default	Status		Default Value										
	Power On Sequence		3900h					Idle mode off					
	SW Reset		The same as above										
	HW Reset		The same as above										
Flow Chart	Idle mode Off IDMON(39h) Idle mode On Host Driver Host Legend Command Parameter Display Action Mode Sequential Transfer												

WRDISBV (5100h): Write Display Brightness

5100H	WRDISBV											
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	W	51h	5100	-	DBV[7:0]							
			5101	-	-	-	-	-	-	-	-	-
Description	This command is used to adjust brightness.											
Restrictio	-											
Default			Status		Default Value							
			Power On Sequence	5100h				00h				
				5101h				00h				
			SW Reset		The same as above							
			HW Reset		The same as above							
Flow Chart	WRDISBV(51h) Parameter DBV[8:0] New brightness is utilized Host Driver Legend Command Parameter Display Action Mode Sequential Transfer											

SCACTRL (6900h): Scaling Up Control

6900H	SCACTRL											
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
SCACTRL	R/W	69	6900	-	-	-	-	-	-	-	D[1:0]	
Description	This command sets operation mode of MIPI clock lane during porch time.											
	Bit	Symbol		Description				Comment				
	D[1:0]	SC_MOD_SEL		Scaling up ratio selection				0= off 1= 2x scaling up 2=1.33x scaling up 3= reserved				
Restrictio	-											
Default	Status			Default Value								
	Power On Sequence			6900h					00h			
	SW Reset			The same as above								
	HW Reset			The same as above								
Flow Chart	SCACTRL(69h) Parameter SC_MOD_SEL[1:0] Scaling up process Host Driver Legend Command Parameter Display Action Mode Sequential Transfer											

IFCONF (6B00h): Interface Configure

6900H	IFCONF											
Instruction	R/W	Address		Parameter								
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0
IFCONF	R/W	6B	6B00	-	-	-	-	D4	-	-	-	-
Description	PORT_1_2_SEL_CMD1: Set MIPI Port1 or Port2 selection. XOR with PORT1_2_SEL (CMD2 page0 B102 D7).											
	Bit	Symbol		Description				Comment				
	D4	PORT1_2_SEL_CMD1		MIPI 1 port or 2 port selection				Refer to the table below				
	PORT_1_2_SEL_CMD1 (CMD1)				PORT1_2_SEL (CMD2 p0)				MIPI Port Selection			
	0h				0h				1-Port			
	0h				1h				2-Port			
	1h				0h				2-port			
1h				1h				1-port				
Restriction	-											
Default	Status			Default Value								
	Power On Sequence			6B00h						10h		
	SW Reset			The same as above								
	HW Reset			The same as above								
Flow Chart	WRCABC(6Bh) Parameter PORT1_2_SEL_CMD1 Port1 or port2 Host Driver Legend Command Parameter Display Action Mode Sequential Transfer											

RESCTRL1 (8000h): Resolution Control1

8000H	RESCTRL1													
Instruction	R/W	Address		Parameter										
		MI	Othe	D1	D7	D6	D5	D4	D3	D2	D1	D0		
RESCTRL1	R/W	80h	8000	-	-	-	-	-	-	-	-	-	D0	
			8001	-	NC[7:0]									
			8002	-	NL[7:0]									
			8003	-	-	-	-	-	NC[8	-	-	-	NL[8	
Description	This command is used to set panel type and display resolution.													
	Bit	Symbol	Description						Comment					
	D0	OSC_FREQ_SEL	OSC frequency selection						0= 69.75MHz 1= 93MHz					
	D[8:0]	NC[8:0]	X-axis resolution						X-axis resolution= NC[8:0]*8					
	D[8:0]	NL[8:0]	Y-axis resolution						Y-axis resolution= NL[8:0]*8					
Restrictio	Resolution switch is only valid in <i>SLPIN</i> mode.													
Default	Status		Default Value											
	Power On Sequence		8000h						01h					
			8001h						40h					
			8002h						40h					
			8003h						11h					
	SW Reset		The same as above											
HW Reset		The same as above												
Flow Chart	RESCTRL1(80h) Parameter GD_HALF OSC_FREQ_SEL NC[8:0] NL[8:0] New Panel Type and Resolution Host Driver Legend Command Parameter Display Action Mode Sequential Transfer													

12 Reliability

No.	Item	Condition	Judgement Criterion
1	High Temperature Storage	80°C 240hrs	After testing 1.No clearly visible defects or remarkable deterioration of display quality. 2.No function-related abnormalities *The results must be checked after 2hours later under room temperature
2	High Temperature Operating	70°C 240hrs	
3	Low Temperature Storage	-40°C 240hrs	
4	Low Temperature Operating	-20°C 240hrs	
5	High Temperature / Humidity Storage	60°C/90%RH 240hrs	
6	High Temperature / Humidity Operating	60°C/90%RH 240hrs	
7	Thermal Shock	-30°C ↔ 80°C, 0.5hr, Change time <1min, 100cycles	
8	ESD	Air discharge ±2kv Contact discharge ±1kv	After testing 1.Hard defect should not happen 2.If it would be recovered to normal state after resetting, it would be judged as a good state.

13 Handling Precautions

13.1 Mounting Method

This Micro-OLED product consists of one silicon backplane and one cover glass, which can easily get damaged. Extreme care should be used when handling the MICRO-OLED.

13.2 Caution of Against Static Charge

For this Micro-OLED, use C-MOS drivers, do not input and signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects Micro-OLED. Against static charge, you should make sure that the product is safe or not by experiment in advance.

13.3 Packing

The packing principle is that Micro-OLED module should keep its packing condition at the time of delivery. For safety & avoiding the module damage, Carton box must stack the below 4 boxes.

When storing the Micro-OLED after unpacking, note the followings. Micro-OLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.

To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

13.4 Caution for Operation

If you do not follow normal POWER ON, OFF sequence or abnormal operating, then Micro-OLED module can be damaged electro-optically and does not recover. Do not change software without SeeYA confirmation.

Micro-OLED module may not display normally when twisting power or pressing power is added. Therefore, you should secure Micro-OLED module maximum thickness at set assembly not to have any pressure affect Micro-OLED module.

Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use MICRO-OLED Module below maximum operating humidity.

Micro-OLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage Micro-OLED module by surrounding elements.

To satisfy EMI standards, you should plan your design after considering emitting energy. We can't guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area. Image-sticking may occur if Micro-OLED displays same image for a long time, so you need to make a change for Micro-OLED.

13.5 Storage

Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity. Store with no contact with polarizer surface. It is recommended to store them as they have been contained in the inner container when we delivered them.

13.6 Safety Precautions

Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMICRO-OLED module, dust adhesion, or scratches on the display part. In the event that the contents of AMICRO-OLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary. Do not use the AMICRO-OLED module for the special purpose besides display units. Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken. For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

13.7 Precautions before use

You should discuss the following case with SeeYA:

- in case of any questions about contents of this "Specification for Approval".
- in case of occurring new problems not mentioned at this "Specification for Approval".
- in case of your request about income inspection specification change.
- in case of occurring new problem at your driving test.

*If SeeYA has to change the conditions specified in the specification, previously shall be held and decided.

14 Warranty

Basically, warranty term is 12 months of reliability characteristics of quality level after the outgoing date in SeeYA, could compensate for defectives which happens within warranty term under condition that the products should be stored or be used as specified under normal condition within the contents of specification.

Otherwise, it is impossible to compensate for defectives when they happen by customer's mistake such as careless handing or circuit change, etc.

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15 Packing

