SeeYA 0.49” Micro-OLED Specification

Model Name: SY049WDM02

Revision

Version	Date	Description
V1.0	2021.4.7	Initial release
V1.1	2021.4.15	Correct Page13 application circuit； Update page53 warranty term to “12months”

Contents

1 General Description

This display is a 0.49 inch diagonal, 1920(RGB) × 1080 dots active matrix color OLED module based on single-crystal silicon transistors. This module integrates panel driver and logic driver, and realizes small size, light weight, low power consumption and high resolution.
Applications: Augmented Reality, View finders, Head mounted displays, etc.

- 1920 x 1080 SPR Resolution
  Multi-Resolution (4*M, M=160~480) x RGB x (4*N, N=120~270)
- Frame rate: 1920x1080 up to 90Hz
- Support 8bits or 10bits color depth
- Interface
  -- MIPI+ I2C
  -- MIPI DPHY v1.2 with one port (4 lanes), 1.0Gbps/Lane
  -- MIPI DSI v1.01 R11 Video mode
  -- Support VESA-DSC v1.1 in-chip decoder (3X and 3.75X compression ratio)
  -- Support scaling up 1.33x(e.g., 1440x810 to 1920x1080), 1.5x (e.g., 1280x720 to 1920x1080) and 2x (e.g., 960x540 to 1920x1080)
- Scan direction selection, up or down and right or left
- Orbit supported
- Wide range Brightness adjustment
- Sequential/Global emission
- Temperature compensation
- Image Anchoring

2 General Feature

Parameter	Specification
Resolution	1920(H) x 1080 (V)
Number of dots	1920x1080x2(2/3 SPR)
Pixel Size	5.616µm x 5.616µm
Active Area	10.783mm x 6.065mm / 0.49'' diagonal
Luminance	1800cd/m² typical
Contrast Ratio	50000:1
Uniformity	> 85%
Operating Voltage	AVDD: 5.3v~5.5v AVEE: -4~-5.5v VDDI: 1.65~1.95v
Power Consumption (3 power mode,90hz,1800nits, VESA on, Rolling mode)	468mW
Gray Levels	256 or 1024
Interface	MIPI
Frame Rate	60Hz~90Hz
Weight	~1g
Operating Temperature	-20°C to +70°C
Storage Temperature	-40°C to +80°C

3 Optical

Symbol	Parameter	Min.	Typ.	Max.	Unit
Brightness	Tpanel=20℃ ~50℃	1350	1800	2250	cd/m2
CR	white to Black Contrast Ratio	20000:1	50000:1		
Uniformity	9 points uniformity	85			%
Red Chromaticity	CIE1931-x	0.625	0.655	0.685	
	CIE1931-y	0.300	0.330	0.360	
Green Chromaticity	CIE1931-x	0.210	0.245	0.280	
	CIE1931-y	0.650	0.680	0.710	
Blue Chromaticity	CIE1931-x	0.120	0.150	0.180	
	CIE1931-y	0.025	0.055	0.085	
White Chromaticity	CIE1931-x	0.298	0.313	0.328	
	CIE1931-y	0.314	0.329	0.343	
Color Gamut	DCI-P3	80%	90%		
View angle	White luminance decay to 50%	35°			
Frame rate		60		90	HZ
Power consumption	90hz,1800nits, VESA DSC on, Full white, No scaling		468	515	mW

Note1: If there is no specified, the specification of optical is specified at 30 degree Celsius.

Note2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. Brightness is measured as peak luminance at full white pattern (Gray level=255);

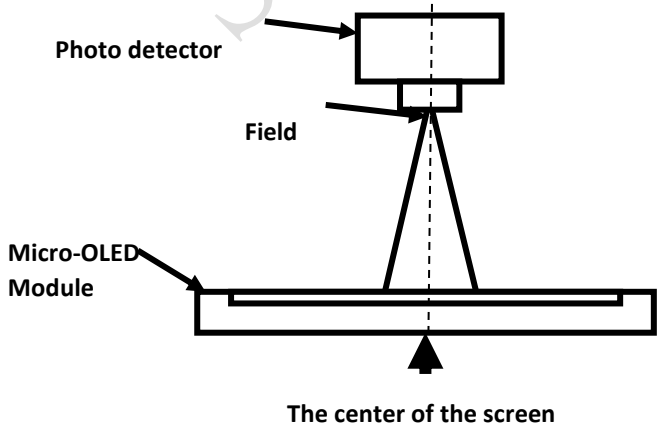


Fig.1

Note3: Definition of Uniformity at highest gray level(255 or 1023) and 100%duty emission.

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

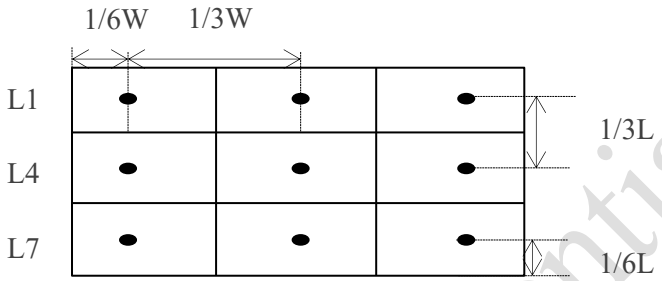
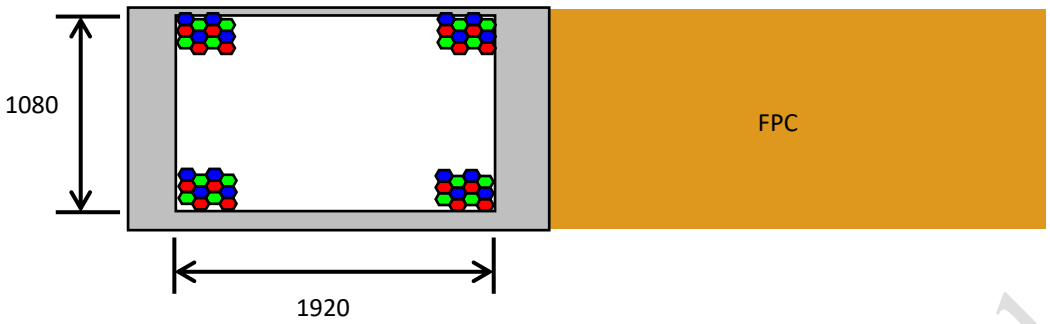


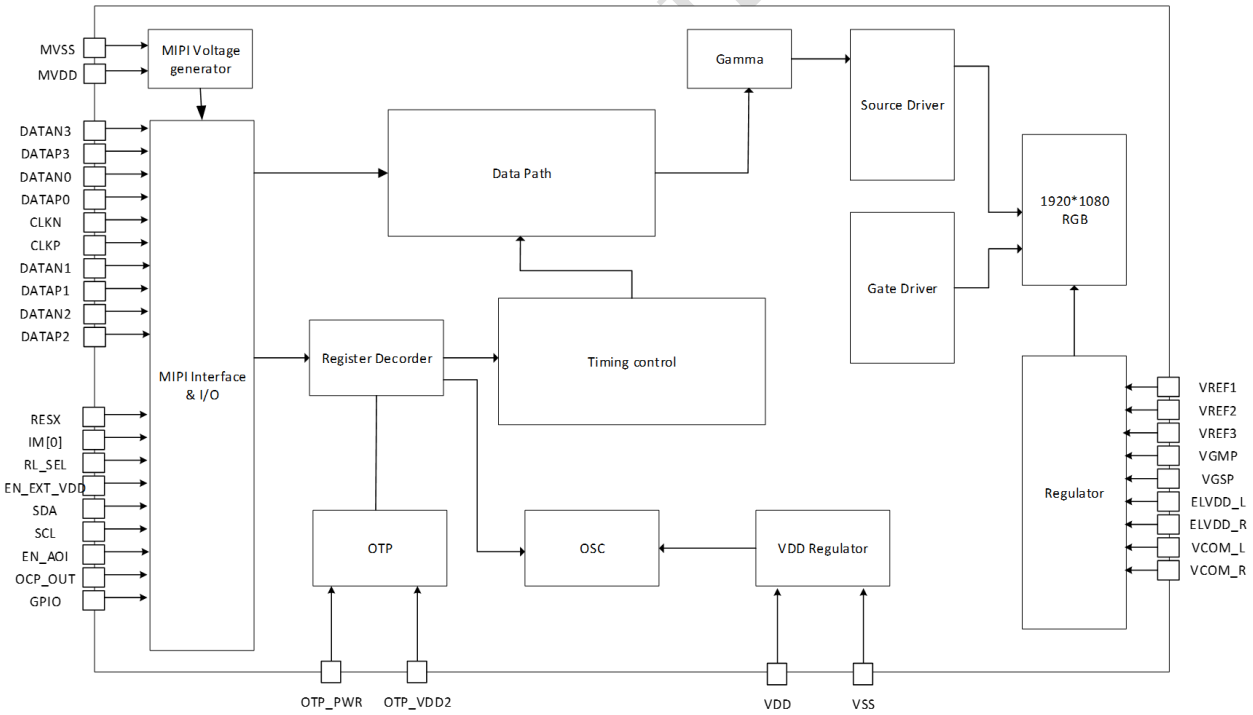
Fig. 2

4 Pixel Arrangement

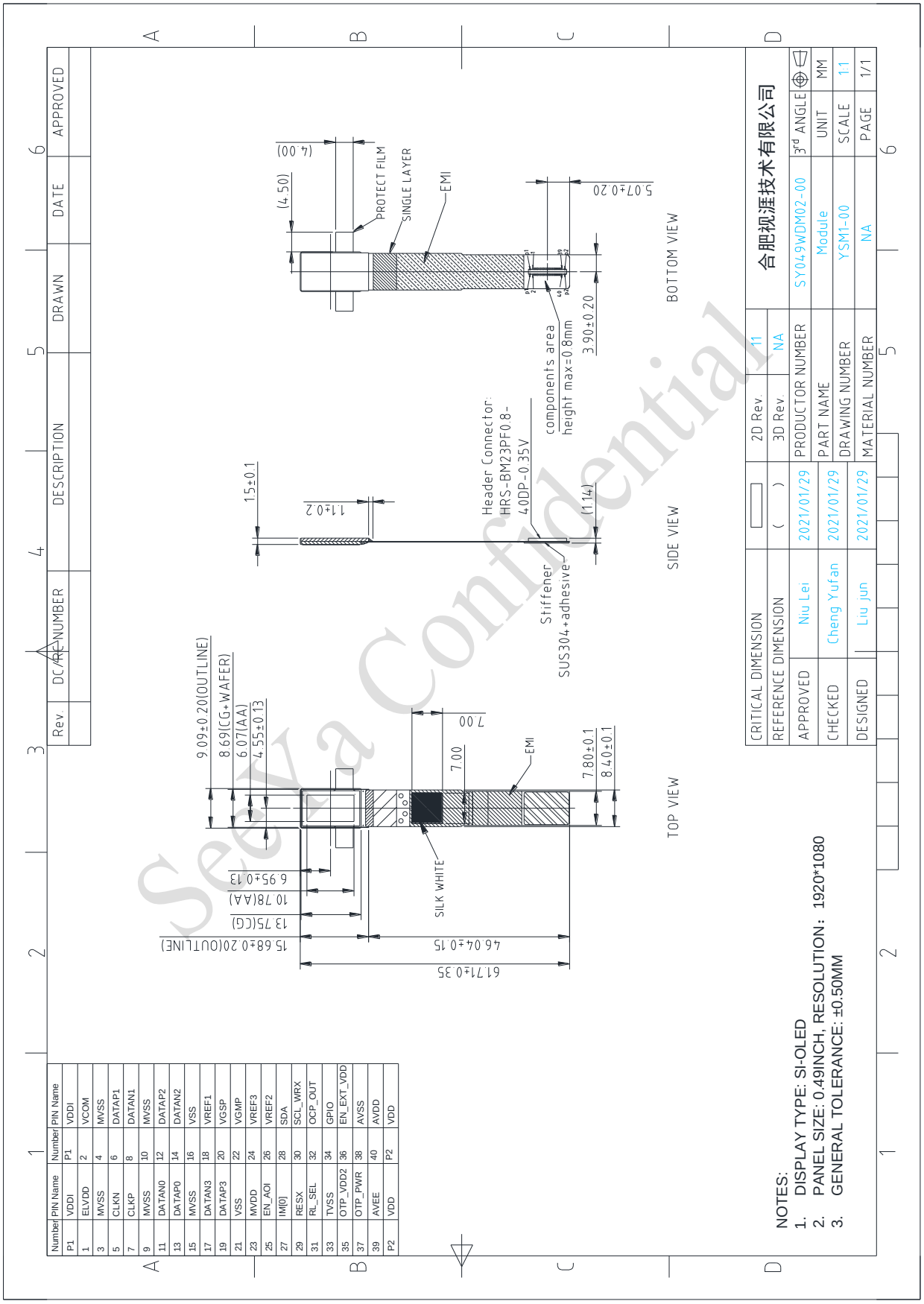


5 System block

System block diagram



6 Module Diagram



Number	PIN Name	Number	PIN Name
P1	VDDI	P1	VDDI
1	ELVDD	2	VCOM
3	MVSS	4	MVSS
5	CLKN	6	DATAP1
7	CLKP	8	DATAN1
9	MVSS	10	MVSS
11	DATAN0	12	DATAP2
13	DATAP0	14	DATAN2
15	MVSS	16	VSS
17	DATAN3	18	VREF1
19	DATAP3	20	VGSP
21	VSS	22	VGMP
23	MVDD	24	VREF3
25	EN_AOI	26	VREF2
27	IM[0]	28	SDA
29	RESX	30	SCL_WRX
31	RL_SEL	32	OCP_OUT
33	TVSS	34	GPIO
35	OTP_VDD2	36	EN_EXT_VDD
37	OTP_PWR	38	AVSS
39	AVEE	40	AVDD
P2	VDD	P2	VDD

7 Pin Description

7.1 Pin Description

Pin No.	Symbol	Type	Description
P1	VDDI	Power	Power supply for interface system except for the interface.
P1	VDDI	Power	Power supply for interface system except for the interface.
1	ELVDD	Output	Power supply for OLED cell. connect a capacitor for stabilization.
2	VCOM	Output	Regulator output for common electrode voltage. connect a capacitor for stabilization, connect a TVS diode to GND.
3	MVSS	Power	System GND for MIPI interface.
4	MVSS	Power	System GND for MIPI interface.
5	CLKN	Input	This pin is DSI CLK- signal if MIPI interface is used. CLKP/N is differential small amplitude signals. If not used, please keep it open.
6	DATAP1	Input/ Output	This pin is DSI D1+ signal if MIPI interface is used. DATA1P/N is differential small amplitude signals. If not used, please keep it open.
7	CLKP	Input	This pin is DSI CLK+ signal if MIPI interface is used. CLKP/N_PTA is differential small amplitude signals. If not used, please keep it open.
8	DATAN1	Input/ Output	This pin is DSI D1- signal if MIPI interface is used. DATA1P/N is differential small amplitude signals. If not used, please keep it open.
9	MVSS	Power	System GND for MIPI interface.
10	MVSS	Power	System GND for MIPI interface.
11	DATAN0	Input/ Output	This pin is DSI D0- signal if MIPI interface is used. DATA0P/N is differential small amplitude signals. If not used, please keep it open.
12	DATAP2	Input/ Output	This pin is DSI D2+ signal if MIPI interface is used. DATA2P/N is differential small amplitude signals. If not used, please keep it open.
13	DATAP0	Input/ Output	This pin is DSI D0+ signal if MIPI interface is used. DATA0P/N is differential small amplitude signals. If not used, please keep it open.
14	DATAN2	Input/ Output	This pin is DSI D2- signal if MIPI interface is used. DATA2P/N is differential small amplitude signals. If not used, please keep it open.
15	MVSS	Power	System GND for MIPI interface.
16	VSS	Power	System GND for internal digital system.
17	DATAN3	Input/ Output	This pin is DSI D3- signal if MIPI interface is used. DATA3P/N is differential small amplitude signals. If not used, please keep it open.
18	VREF1	Power	Regulator output for internal reference voltage. Connect a capacitor for stabilization.
19	DATAP3	Input/ Output	This pin is DSI D3+ signal if MIPI interface is used. DATA3P/N is differential small amplitude signals. If not used, please keep it open.
20	VGSP	Output	Regulator output for gamma low voltage generation. Connect a capacitor for stabilization.
21	VSS	Power	System GND for internal digital system.
22	VGMP	Output	Regulator output for gamma high voltage generation. Connect a capacitor for stabilization.
23	MVDD	Output	Regulator output for MIPI digital system power. Connect a capacitor for stabilization.
24	VREF3	Output	Regulator output for internal reference voltage. Connect a capacitor for stabilization. Connect a Schottky diode to GND
25	EN_AOI	Input	Connect to GND.
26	VREF2	Output	Regulator output for internal reference voltage. Connect a capacitor for stabilization.

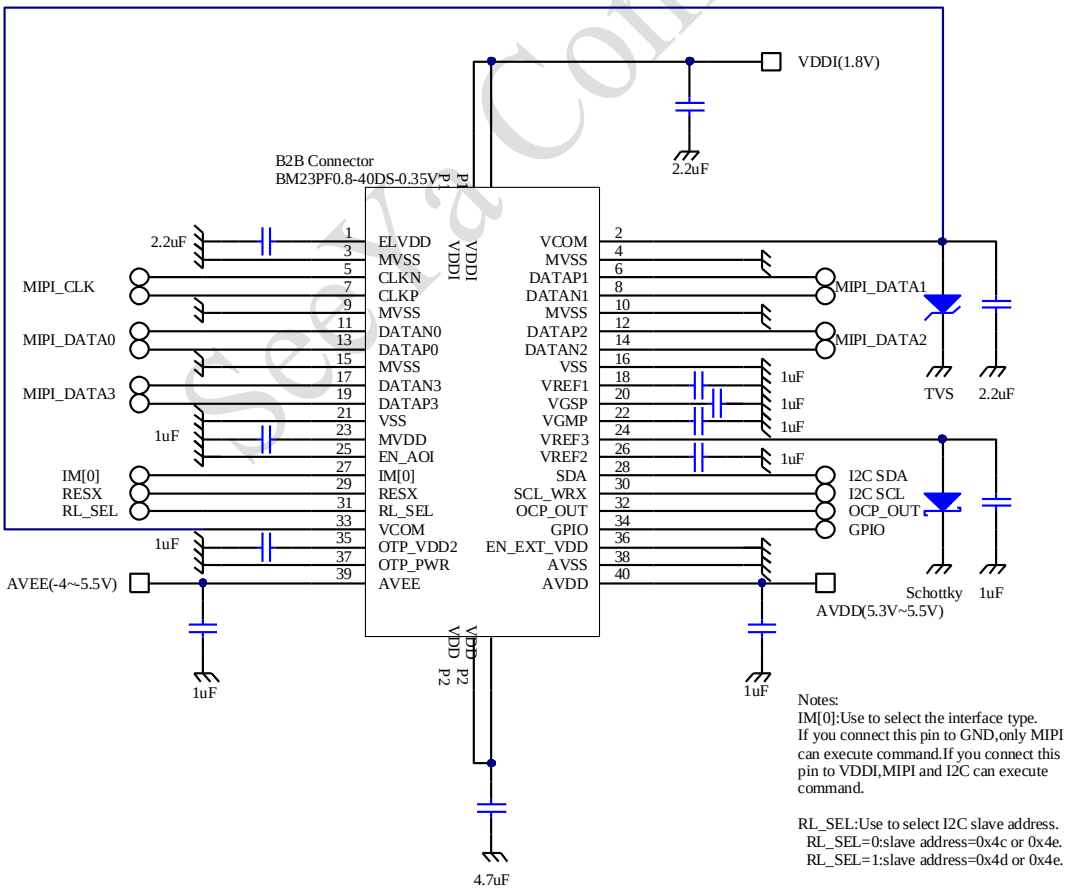
<table>
<tr><td>27</td><td>IM[0]</td><td>Input</td><td>Use to select the Interface type.<table><tr><td>IM[0]</td><td>Command</td><td>Display Data</td></tr><tr><td>0V</td><td>MIPI</td><td>MIPI</td></tr><tr><td>1.8V</td><td>I2C or MIPI</td><td>MIPI</td></tr></table></td></tr>
<tr><td>28</td><td>SDA</td><td>Input/ Output</td><td>Bi-direction data PIN in I2C I/F.
If this pin is not used, please connect to VDDI.</td></tr>
<tr><td>29</td><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>30</td><td>SCL_WRX</td><td>Input</td><td>Synchronous clock signal in I2C I/F.
If this pin is not used, please connect to VDDI.</td></tr>
<tr><td>31</td><td>RL_SEL</td><td>Input</td><td>Use to select I2C slave address.
RL_SEL = 0v: slave address = 0x4C or 0x4E.
RL_SEL = 1.8v: slave address = 0x4D or 0x4E.</td></tr>
<tr><td>32</td><td>OCP_OUT</td><td>Output</td><td>Over current protect output flag.</td></tr>
<tr><td>33</td><td>V_TEST</td><td>Output</td><td>Connect to VCOM.</td></tr>
<tr><td>34</td><td>GPIO</td><td>Input/ Output</td><td>Digital global purpose in/out test pin.</td></tr>
<tr><td>35</td><td>OTP_VDD2</td><td>Output</td><td>Regulator output for MTP analog system power.
Connect a capacitor for stabilization.</td></tr>
<tr><td>36</td><td>EN_EXT_VDD</td><td>Input</td><td>Connect to GND.</td></tr>
<tr><td>37</td><td>OTP_PWR</td><td>Input</td><td>Connect to GND.</td></tr>
<tr><td>38</td><td>AVSS</td><td>Power</td><td>System GND for analog system.</td></tr>
<tr><td>39</td><td>AVEE</td><td>Power</td><td>-4.0V~-5.5V Power supply for OLED cell.
connect a capacitor for stabilization.</td></tr>
<tr><td>40</td><td>AVDD</td><td>Power</td><td>5.3V~5.5V Power supply for analog system.
connect a capacitor for stabilization.</td></tr>
<tr><td>P2</td><td>VDD</td><td>Output</td><td>Regulator output for logic system power.
Connect a capacitor for stabilization.</td></tr>
<tr><td>P2</td><td>VDD</td><td>Output</td><td>Regulator output for logic system power.
Connect a capacitor for stabilization.</td></tr>
</table>

7.2 Application circuit

Below table is the instruction of peripheral circuit. Regarding power supply capacitor connections, mount an appropriate capacitor for each power supply.

No.	Signal Name	Typical Value	Maximum Rated Voltage	Note
1	VDDI	Cap, 2.2uF	6.3V	-
2	AVDD	Cap, 1.0uF	10V	-
3	ELVDD	Cap, 2.2uF	10V	-
4	AVEE	Cap, 1uF	10V	-
5	VDD	Cap, 4.7uF	6.3V	-
6	MVDD	Cap, 1uF	6.3V	-
7	VGMP	Cap, 1uF	10V	-
8	VGSP	Cap, 1uF	10V	-
9	VREF1	Cap, 1uF	6.3V	-
10	VREF2	Cap, 1uF	6.3V	-
11	VREF3	Cap, 1uF Schottky Diode	6.3V	
12	VCOM	Cap, 2.2uF TVS	10V	Recommend: TVS VBR min>8V
13	OTP_VDD2	Cap, 1uF	6.3V	-
14	TVSS	Res , 0 Ω	-	-

Below circuit is one of typical example for reference to drive the module with D-PHY.



8 Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When this Micro-OLED product is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended to use this Micro-OLED product within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this Micro-OLED product will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	5.5	V
Power Supply Voltage (2)	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
Power Supply Voltage in AOI mode	VDDI	1.32	V
	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
MIPI Differential Input	CLKP, CLKN DATAP0, DATAN0 DATAP1, DATAN1 DATAP2, DATAN2 DATAP3, DATAN3	1.32	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI+0.3	V
Operating temperature	Topr	-20 ~ 70	°C
Storage temperature	Tstg	-40 ~ 80	°C

8.2 DC Characteristic

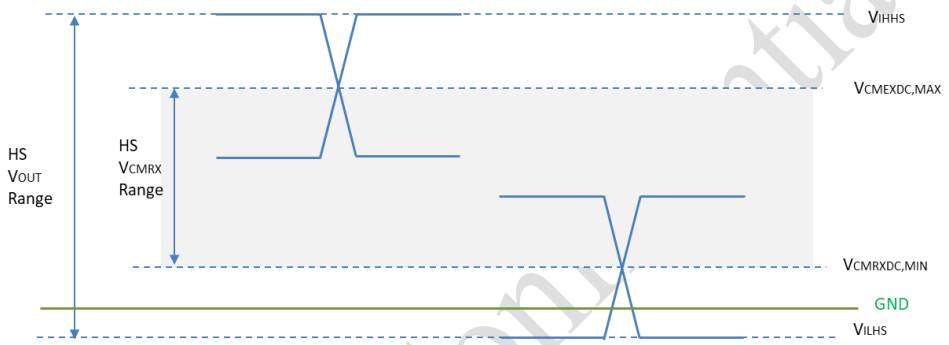
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage						
AVDD Input Level	AVDD	-	5.3		5.5	V
Digital I/O Power Supply (non-MIPI I/O)	VDDI	-	1.65	1.8	1.95	V
Digital I/O Input Level @Logic High	VIH	VDDI=1.65V ~ 1.95V	0.7*VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	VIL	VDDI=1.65V ~ 1.95V	0	-	0.3*VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1mA	0.8*VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1mA	0	-	0.2*VDDI	V
Digital I/O Input leakage @Logic High	IIHD	Vin = VDDI			1	uA
Digital I/O Input leakage @Logic Low	IILD	Vin = 0	-1			uA

8.3 DSI DC/AC Characteristic

8.3.1 Receiver characteristic

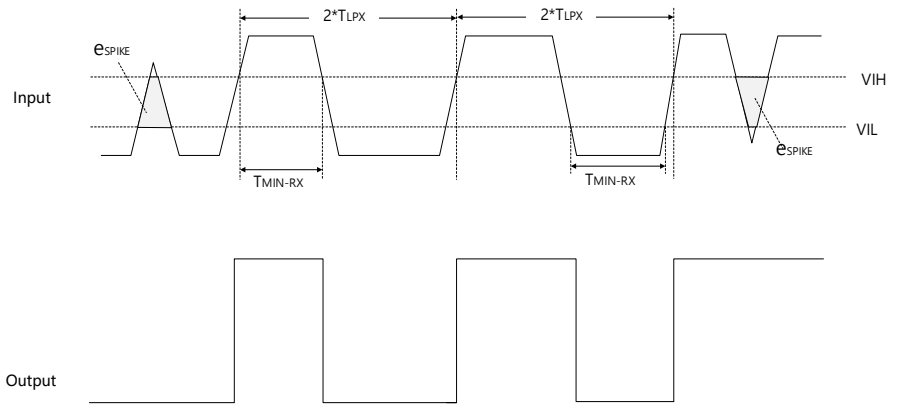
High speed receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IDTH}	Differential input high threshold	-	-	70	mV
V_{IDTL}	Differential input low threshold	-70	-	-	mV
V_{IHHS}	Single-ended input high voltage	-	-	460	mV
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV
C_{CM}	Common-mode termination	-	-	60	pF



Low power receiver characteristic

Parameter	Description	Min	Typ.	Max	Unit
V_{IH}	Logic 1 input voltage	880	-	-	mV
V_{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV
V_{IL_ULPS}	Logic 0 input voltage, ULP state	-	-	300	mV
V_{HYST}	Input hysteresis	25	-	-	mV
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps
T_{MIN-RX}	Minimum pulse width response	20	-	-	



8.3.2 Transmitter Characteristics

High-Speed Transmitter Characteristics

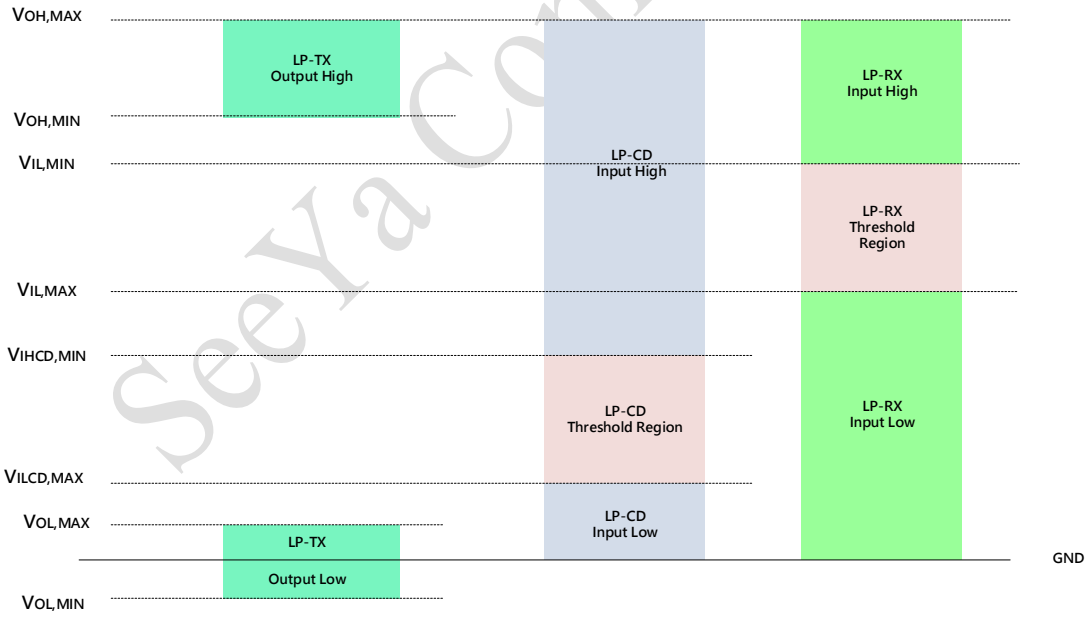
Parameter	Description	Min	Typ.	Max	Unit
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	-	-	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
t_R and t_F (note1,2)	20%-80%rise time and fall time	-	-	0.3	UI
		-	-	0.35	UI

Note:

1. Applicable when supporting maximum HS bitrates ≤ 1Gbps (UI≥1ns)

Low-Power Transmitter Characteristics

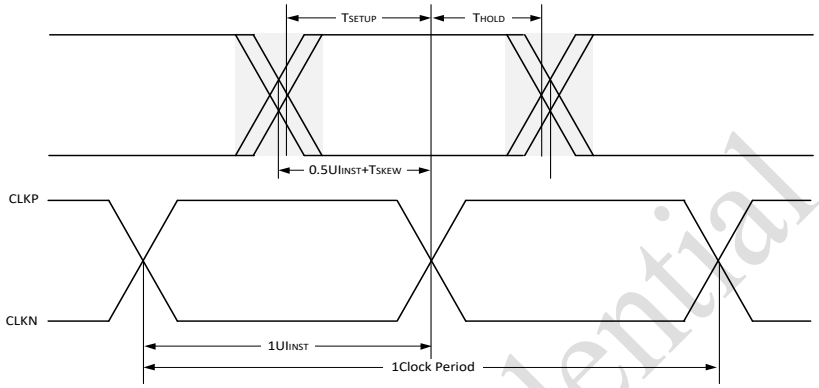
Parameter	Description	Min	Typ.	Max	Unit
V_{OH}	The output high level	1.1	1.2	1.3	V
V_{OL}	The output low level	-50	-	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω
V_{IHCD}	Logic1 contention threshold	450	-	-	mV
V_{ILCD}	Logic0 contention threshold	-	-	200	mV



8.4 Timing Characteristics

8.4.1 High Speed Mode Characteristics

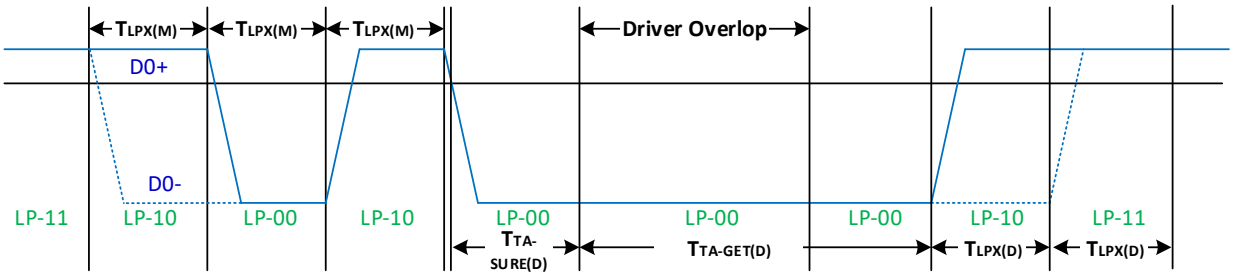
Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS



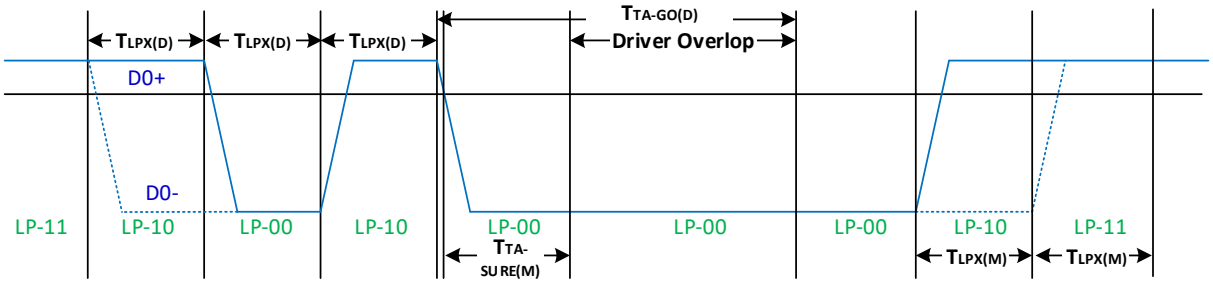
8.4.2 Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state(LP-00) during a Link Turnaround	T_{LPX}	-	$2*T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround	$5* T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	$4* T_{LPX}$			

- Bus Turnaround from MPU to display module



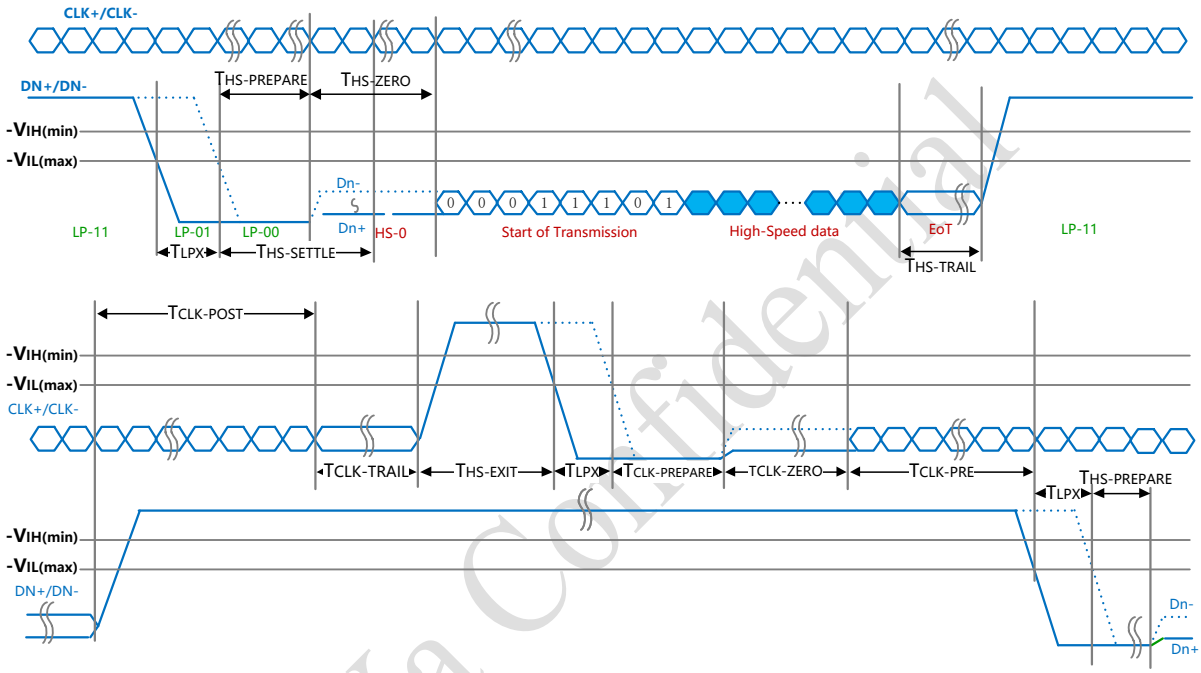
- Bus Turnaround from MPU to display module



8.4.3 High Speed Mode Operation Timing Characteristics

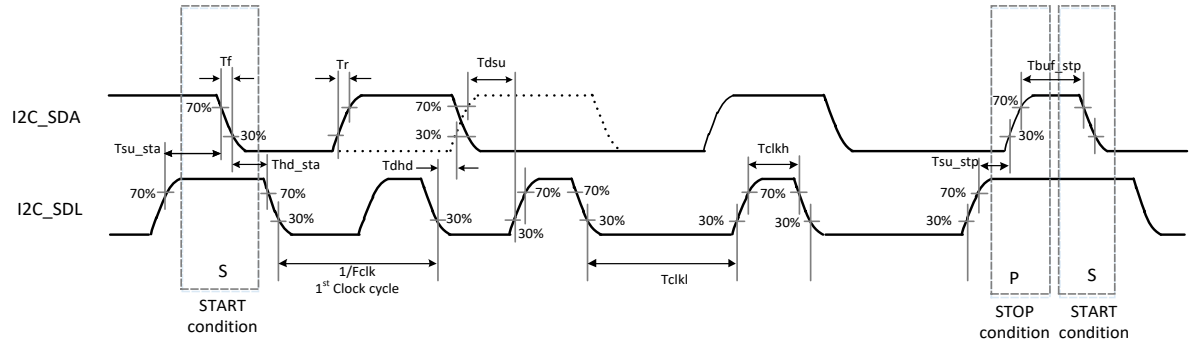
Parameter	Description	Min	Typ.	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL	60ns+52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE	95	-	300	ns
$T_{CLK-TERM\_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst t	60	-	-	ns
$T_{CLK-PREPARE}$+$T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
T_{D-TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX	-	-	35ns+ 4*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns+4*UI	-	85ns+ 6*UI	ns
$T_{HS-PREPARE}$+T_{HS-}	THS-PREPARE + time that the transmitter	145ns+10*	-	-	ns

ZERO	drives the HS-0 state prior to transmitting the Sync sequence	UI			
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value. value.	85ns+6*UI	-	145ns +10*UI	ns



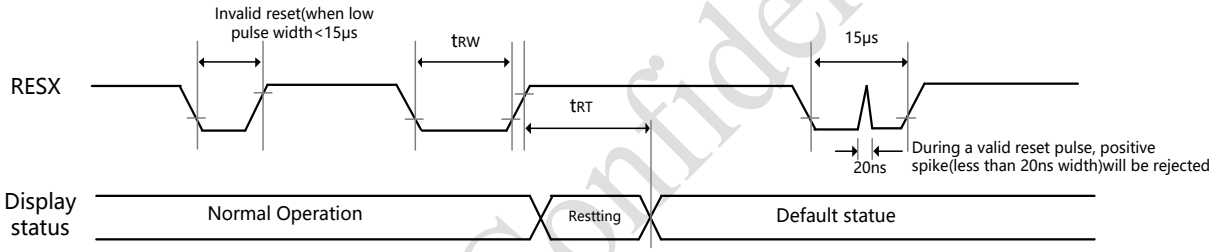
8.4.4 I2C-Bus Interface Timing

Parameter	Symbol	Min.	Ty	Max.	Unit	Conditi
I2C Clock Frequency	F_{clk}	-	-	400	kHz	
I2C Clock Low	Tclkl	1300	-	-	ns	
I2C Clock High	Tclkh	600	-	-	ns	
I2C Data Rising Time	Tdr	-	-	300	ns	
I2C Data Falling Time	Tdf	-	-	300	ns	
I2C Data Setup Time	Tdsu	100	-	-	ns	
I2C Data Hold Time	Tdhd	-	-	TBD	ns	
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns	
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns	
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns	
I2C Bus Free Time (Stop Condition)	Tbuf_stp	1300	-	-	ns	



8.5 Reset Timing Characteristics

When Reset happens in Sleep-out mode, this Micro-OLED product will enter blanking sequence with the maximum time 120 msec. Then this Micro-OLED product will remain in blanking state and return \ default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.

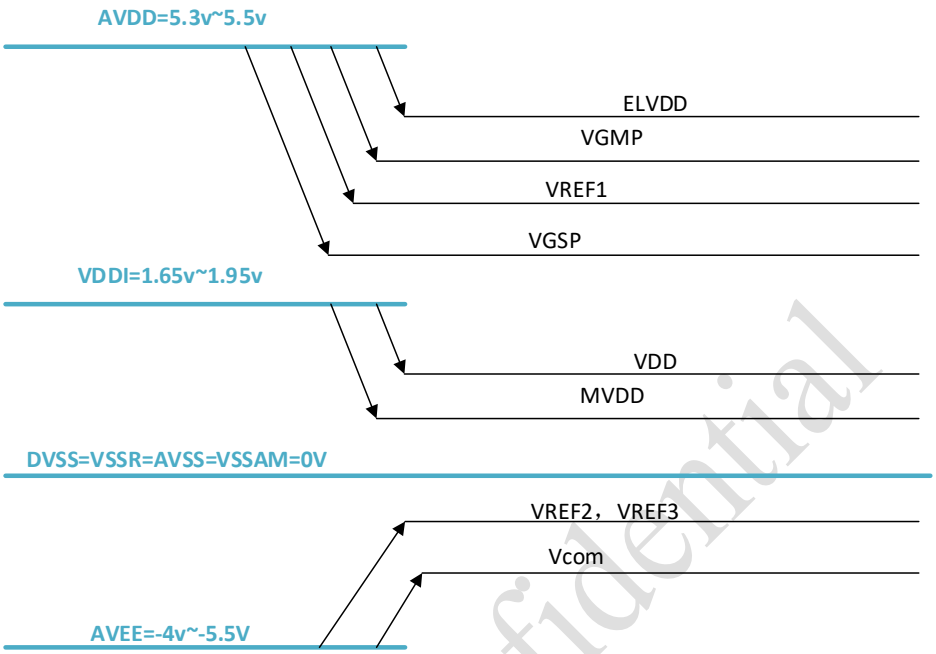


Reset time @VDDI=1.65V to 1.95V, AVSS = VSS = MVSS = 0V, Ta=-40°C to 85°C

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RESX	tRW	Reset low pulse width	15			us	
	tRT	Reset Complete time			20	ms	When reset applied at sleep-in mode
					120	ms	When reset applied at sleep-out mode

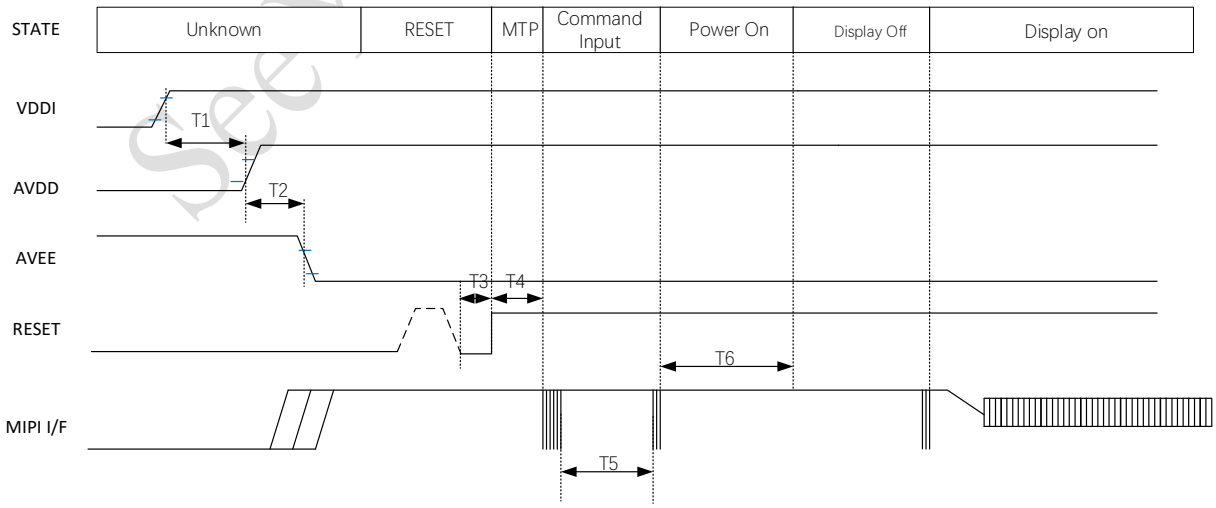
9 Power Generation

9.1 Power Generation Scheme

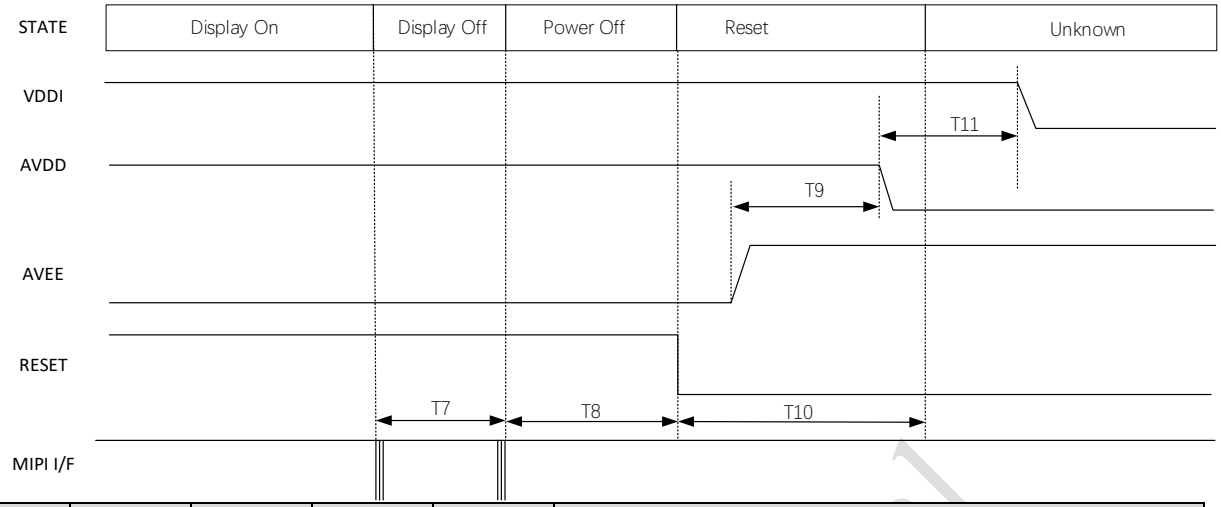


9.2 Power Sequence

Power on sequence



Power off sequence



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between VDDI and AVDD
T2	2	-	-	ms	Power on time between AVDD and AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	OTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	uS	Power on sequence, the period can be modified
T7	1	-	-	uS	Blanking region
T8	-	1	-	uS	Power off sequence, the period can be modified
T9	2	-	-	ms	Power off time between AVEE and AVDD
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVDD and VDDI

10 Interface

This Micro-OLED product supports MIPI interface and inter-integrated circuit interface (I2C). MIPI or I2C is selected by IM0, the detail interface selection by IM0 pin shows in below table.

IM0	Command Execute	Image Write
0	MIPI	MIPI
1	I2C or MIPI	MIPI

10.1 I2C Interface

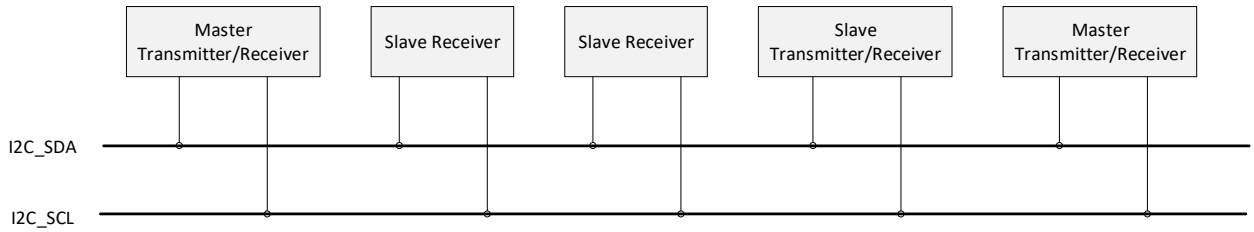
The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte maybe sent. The master generates all clock pulses, including the ninth acknowledge clock pulse.

10.1.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition

- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.



10.1.2 Write Sequence

This Micro-OLED product supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

(1) Data transfer for register writing should follow the format shown as below.

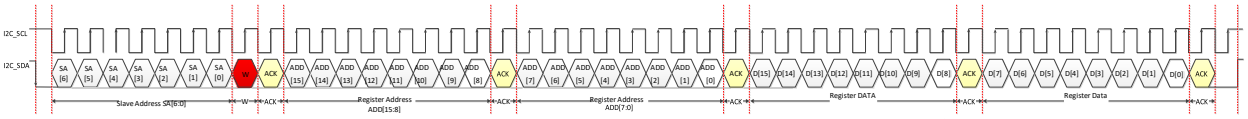
(2) After the START condition, a slave address is sent. R/$\overline{W}$ bit is setting to “0” for Write.

(3) The slave issues an ACK to the master.

(4) 8-bits register address transfer first then transfer the register data parameter.

(5) A data transfer is always terminated by a STOP condition.

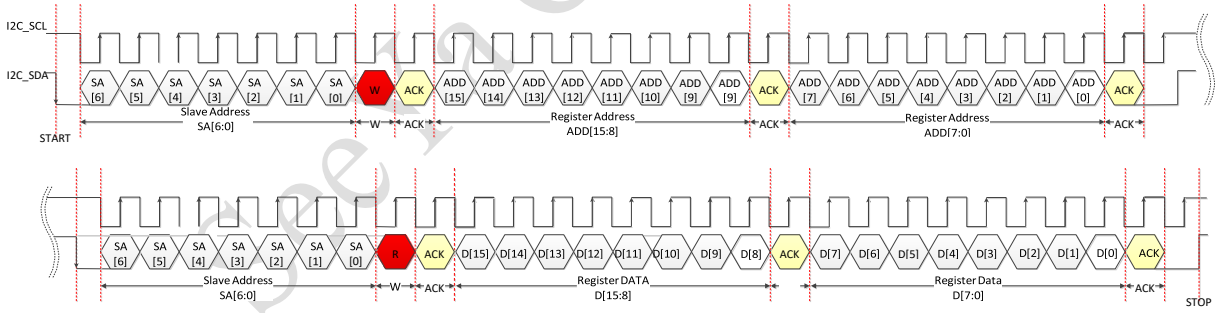
(6) The chip SA [6:0] =1001100.



W: Write Bit, W= “1” here, R: Read Bit,R= “0” here
ACK: Acknowledge Bit, ACK= “0” here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data

10.1.3 Read Sequence

This Micro-OLED product supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W: Write Bit, W= “0” here, R: Read Bit,R= “1” here
ACK: Acknowledge Bit, ACK= “0” here
SA[6:0]: Slave Address
ADD[15:0]: Register Address
D[15:0]: Register Data
NACK: Negative Acknowledge Bit, NACK= “1” here

10.2 MIPI Interface

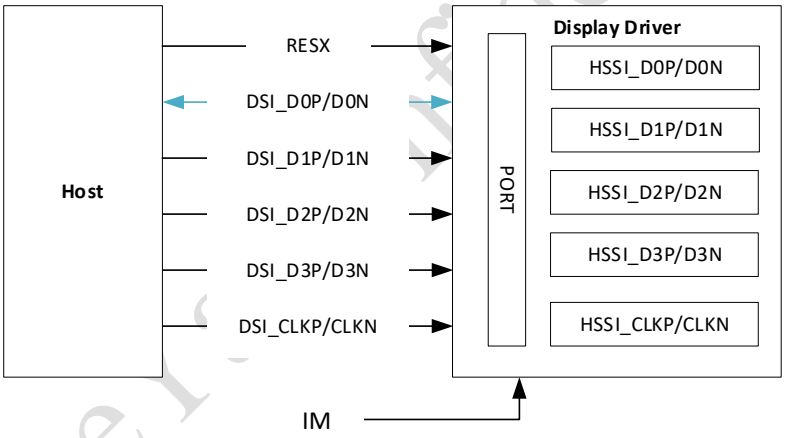
Display serial interface (DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set. The detail Lane configuration for DPHY are listed below.

There are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and this Micro-OLED product shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

10.2.1 DSI System Configuration

This Micro-OLED product supports MIPI 1 port with 2, 3 or 4 lane configurations for DPHY. The system configuration is shown as the figure below. There are HW pin(IM) and registers (Lane_num_cfg, PSWAP, DSWAP) which can set the interface and lane related configuration.



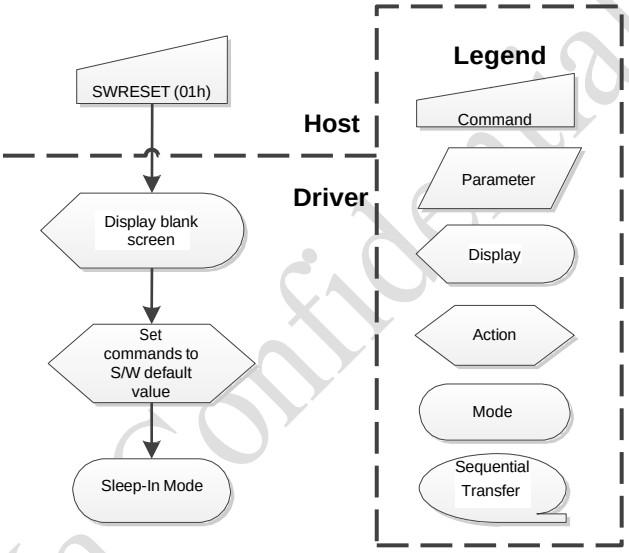
Multi-Lane Distribution and Merging

11 User Command

Command list

Instruction	R/W	Address		D7	D6	D5	D4	D3	D2	D1	D0	Default
		MIPI	Non-MIPI									
SWRESET	W	01h	0100h	No Parameter								N/A
CMODE	R/W	03h	0300h	-	-	-	-	-	-	-	CMODE	80h
SLPIN	W	10h	1000h	No Parameter								N/A
SLPOUT	W	11h	1100h	No Parameter								N/A
ALLPOFF	W	22h	2200h	No Parameter								N/A
ALLPON	W	23h	2300h	No Parameter								N/A
DSPOFF	W	28h	2800h	No Parameter								N/A
DSPON	W	29h	2900h	No Parameter								N/A
CASET	R/W	2Ah	2A00h	XS1[15:8]								00h
	R/W		2A01h	XS1[7:0]								00h
RASET	R/W	2Bh	2B00h	YS1[15:8]								00h
	R/W		2B01h	YS1[7:0]								00h
RAMWR	R/W	2Ch	2C00h	D7	D6	D5	D4	D3	D2	D1	D0	00h
			2C01h	D7	D6	D5	D4	D3	D2	D1	D0	00h
			2C02h	D7	D6	D5	D4	D3	D2	D1	D0	00h
RAMRD	R	2Eh	2E00h	D7	D6	D5	D4	D3	D2	D1	D0	00h
			2E01h	D7	D6	D5	D4	D3	D2	D1	D0	00h
			2E02h	D7	D6	D5	D4	D3	D2	D1	D0	00h
MADCTL	R/W	36h	3600h	-	-	-	-	RGB	-	RSMX	RSMY	00h
IDMOFF	R/W	38h	3800h	No Parameter								N/A
IDMON	R/W	39h	3900h	No Parameter								N/A
COLMOD	R/W	3Ah	3A00h	VIPF[3:0]				IFPF[3:0]				77h
WRDISBV	W	51h	5100h	DBV[7:0]								00h
	W		5101h	-	-	-	-	-	-	-	DBV[8]	00h
SCACTRL	W	69h	6900h							SC_MOD_SEL[1:0]		00h
IFCONFG	R/W	6Bh	6B00h	-	-	-	-	-	-	Lan_num_cfg_CMD1 [1:0]		00h
ANCTRL1	R/W	90h	9000h	-	-	-	-	-	-	-	EN_ANC	00h
ANCTRL1	R/W	91h	9100h	-	-	-	XS_ANC_SHT_DIR	-	XS_ANC_SHT[10:8]			00h
	R/W		9101h	XS_ANC_SHT[7:0]								00h
	R/W		9102h	-	-	-	YS_ANC_SHT_DIR		YS_ANC_SHT[10:8]			00h
	R/W		9103h	YS_ANC_SHT[7:0]								00h

SWRESET(0100h): Software Reset

<table>
<tr><td>0100H</td><td colspan="12">SWRESET</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="10">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SWRESET</td><td>W</td><td>01h</td><td>0100h</td><td>-</td><td colspan="8">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">When the Software Reset command is executed, all related register and parameters are reset to their S/W Reset default values.</td></tr>
<tr><td>Restriction</td><td colspan="12">It is necessary to wait 10m sec to send any command following the S/W Reset.
If S/W Reset is executed in Sleep-out mode, it is necessary to wait 120m sec to send Sleep-Out command. The Software Reset command cannot be sent during Sleep-Out sequence. Any new command cannot be sent within 8-frame until device enters Sleep-In mode.</td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td>Power On Sequence</td><td>0100h</td><td>N/A</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

CMODE(0300h): Compression Mode

0400H	RDID123										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
CMODE	R/W	03h	0300h	-	-	-	-	-	-	-	-	CMODE
Description	These commands are used for compression mode											
Restriction	-											
Default												

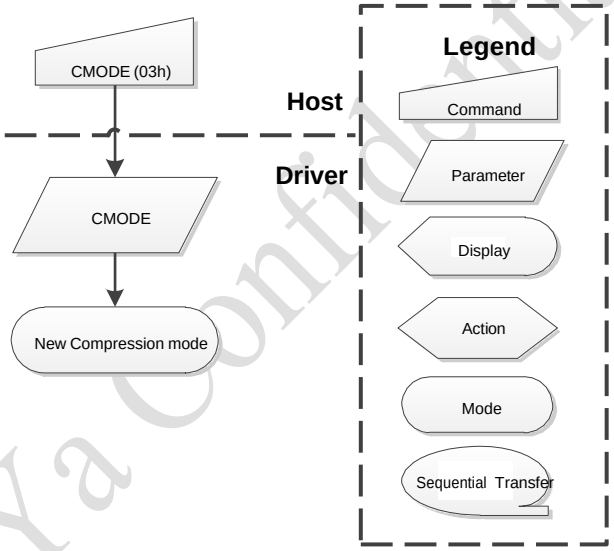
Description:

Bit	Symbol	Description	Comment
D0	CMODE	Enable/Disable compression mode	0=Disable 1=Enable

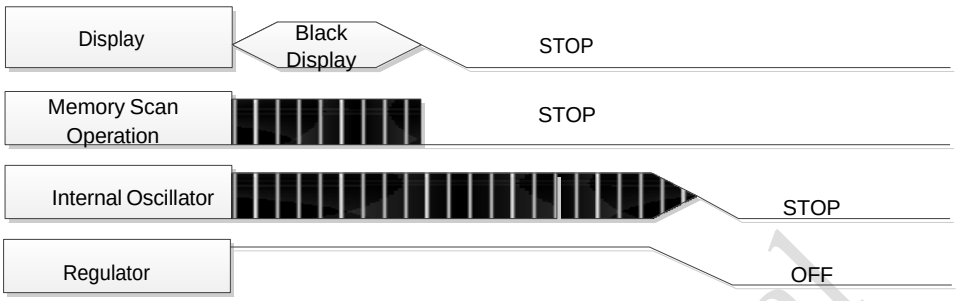
Default:

Status	Default Value	
Power On Sequence	0300h	80h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart:

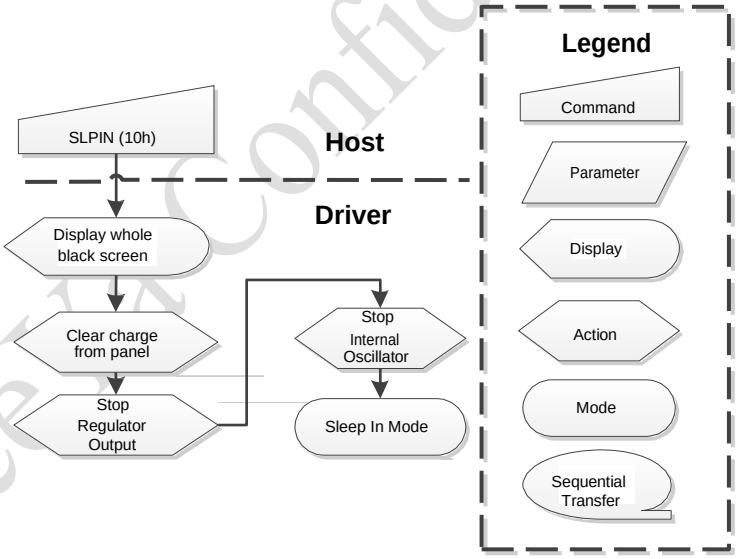


SLPIN (1000h): Sleep In

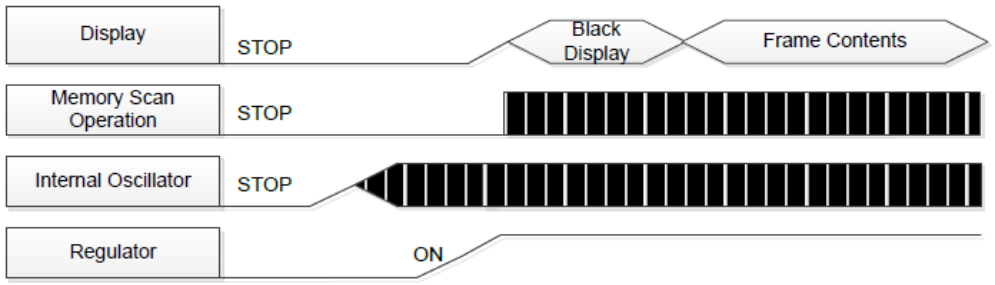
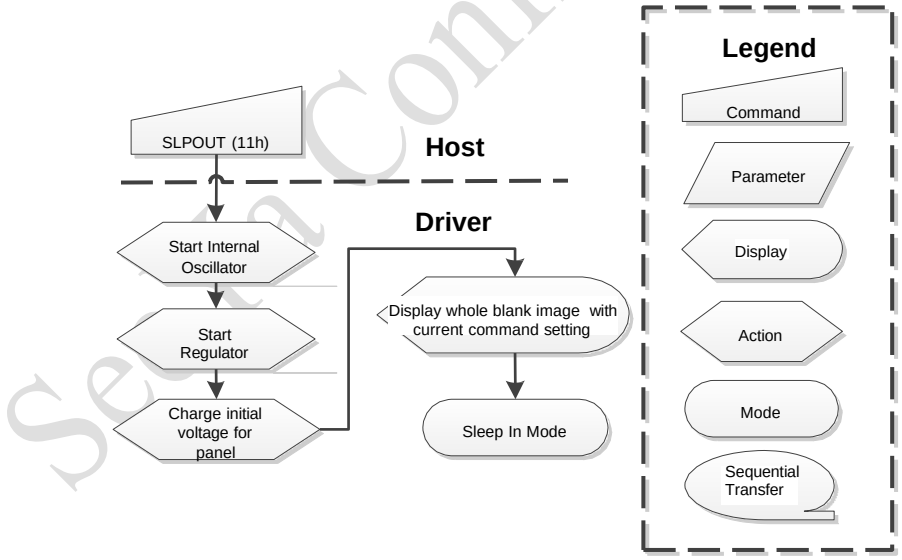
1000H	SLPIN											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	W	10h	1000h	-	No Parameter							
Description	This command force display module to enter *Sleep-In* mode. Under *Sleep-In* mode, internal display oscillator, and panel scanning are all stopped. The interface and related registers are still working and keeps its values. 											
Restriction	-											

Default	Status	Default Value	
	Power On Sequence	1000h	Sleep In Mode
	SW Reset	The same as above	
	HW Reset	The same as above	

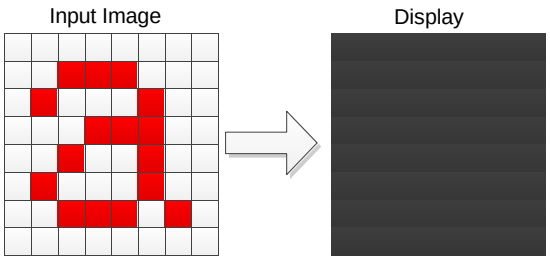
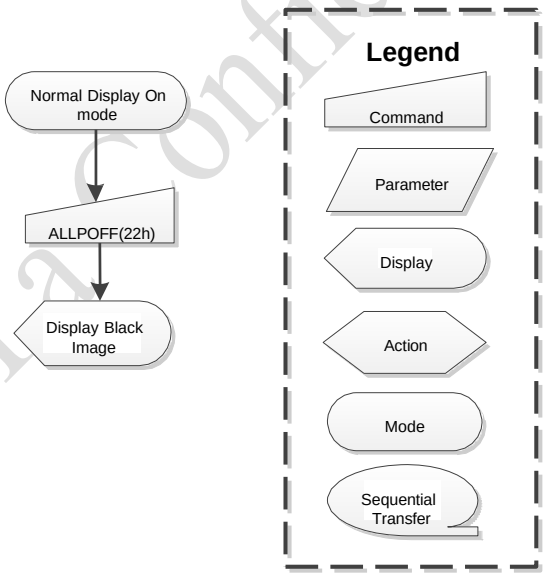
Flow Chart



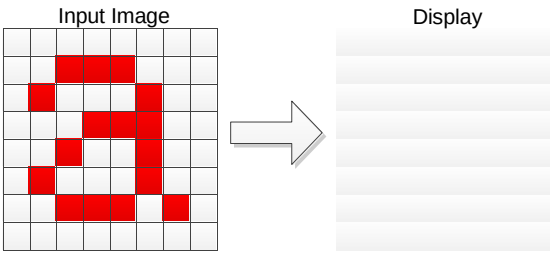
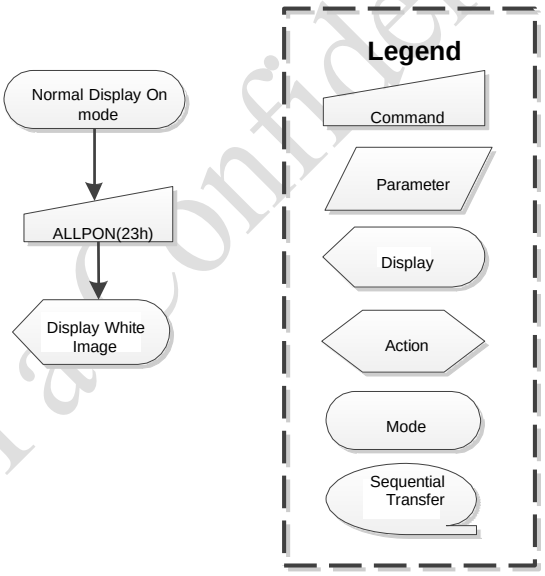
SLPOUT (1100h): Sleep Out

1100H	SLPOUT											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	W	11h	1100h	-	No Parameter							
Description	This command force display module to exit *Sleep-In* mode. Under *Sleep-out* mode regulator, internal display oscillator, and panel scanning are allenable. 											
Restriction	-											
Default	Status	Default Value										
	Power On Sequence	1100h	Sleep In Mode									
	SW Reset	The same as above										
	HW Reset	The same as above										
Flow chart												

ALLPOFF (2200h): All Pixels OFF

2200H	ALLPOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
ALLPOFF	W	22h	2200h	-	No Parameter							
Description	This command forces the display module to display black image in *Display-On* Mode. 											
Restriction	-											
Default	Status	Default Value										
	Power On Sequence	2200h	All Pixel Off									
	SW Reset	The same as above										
	HW Reset	The same as above										
Flow Chart												

ALLPON (2300h): All Pixel ON

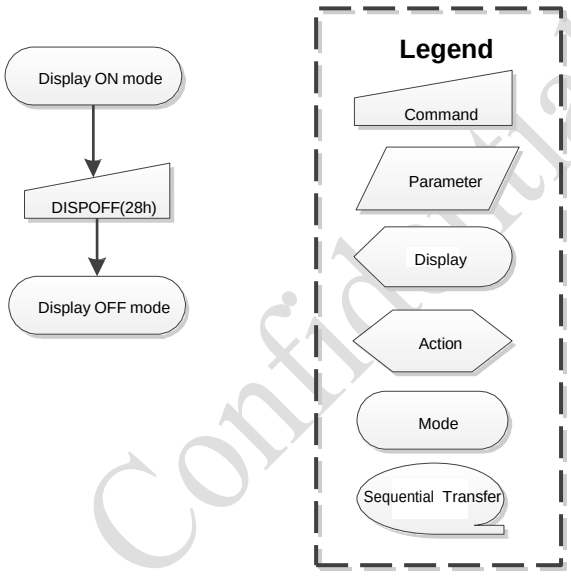
2300H	ALLPON										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
ALLPON	W	23h	2300h	-	No Parameter							
Description	This command forces the display module to display white image in *Display-On* Mode. 										
Restriction	-										
Default	Status	Default Value									
	Power On Sequence	2300h	All Pixel On								
	SW Reset	The same as above									
	HW Reset	The same as above									
Flow Chart											

DISPOFF (2800h): Display OFF

2800H	DISPOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	W	28h	2800h	-	No Parameter							
Description	This command forces the display module to stop displaying image data.											
Restriction	This command has no effect when display driver is already in *DISPLAY-OFF* mode											

Default	Status	Default Value	
	Power On Sequence	2800h	Display Off
	SW Reset	The same as above	
	HW Reset	The same as above	

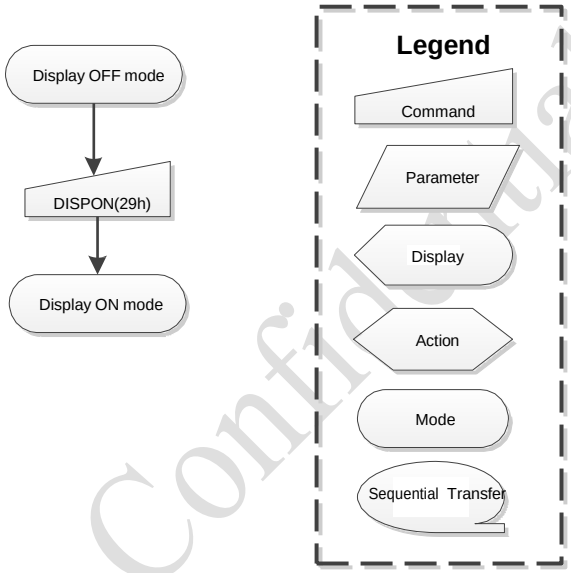
Flow Chart



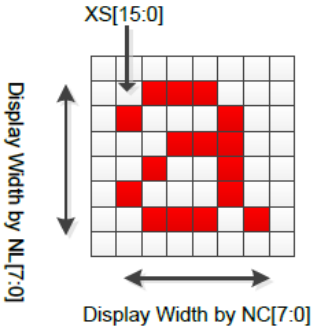
DISPON (2900h): Display ON

2900H	DISPON											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	W	29h	2900h	-	No Parameter							
Description	This command forces the display module to start displaying image data.											
Restriction	This command has no effect when display driver is already in *DISPLAY-ON* mode.											

Default	Status	Default Value	
	Power On Sequence	2900h	Display On
	SW Reset	The same as above	
	HW Reset	The same as above	



CASET (2A00h): Column Address Set

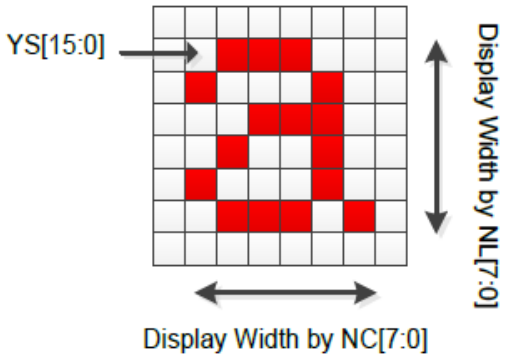
<table>
<tr><td>2A00H</td><td colspan="11">CASET</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="2">CASET</td><td rowspan="2">R/W</td><td rowspan="2">2Ah</td><td>2A00h</td><td>-</td><td colspan="8">XS[15:8]</td></tr>
<tr><td>2A01h</td><td>-</td><td colspan="8">XS[7:0]</td></tr>
<tr><td>Description</td><td colspan="11">This command indicates display start position of display module in columns.
XS[15:0]: Display line start position.
 
</td></tr>
<tr><td>Restriction</td><td colspan="11">1. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, PIXEL_SHIFT_Y_COUNT, XS_ANC_SHT, and YS_ANC_SHT.
2. When anchor shift function is enable(EN_ANC=1), XS have no constraint.
3. When anchor shift function is disable(EN_ANC=0), XS have constraints as below:
a) PIXEL_SHIFT_X_DIR=0(Left)
Parameter range= 0 ⩽ XS[15:0]*1.5 + NC[8:0]*4 - PIXEL_SHIFT_X_COUNT*1.5 ⩽ 1944
b) PIXEL_SHIFT_X_DIR=1(Right)
Parameter range= 0 ⩽ XS[15:0]*1.5 + NC[8:0]*4 + PIXEL_SHIFT_X_COUNT*1.5 ⩽ 1944</td></tr>
<tr><td>Default</td><td colspan="11"><table>
<tr><td>Status</td><td colspan="2">Default Value</td></tr>
<tr><td rowspan="2">Power On Sequence</td><td>2A00h</td><td>00h</td></tr>
<tr><td>2A01h</td><td>00h</td></tr>
<tr><td>SW Reset</td><td colspan="2">The same as above</td></tr>
<tr><td>HW Reset</td><td colspan="2">The same as above</td></tr>
</table></td></tr>
</table>

RASET (2B00h): Row Address Set

2A00H	CASET											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RASET	R/W	2Bh	2B00h	-	YS[15:8]							
			2B01h	-	YS[7:0]							

Description

This command indicates display start position of display module in rows.
XS[15:0]: Display line start position.



Restriction

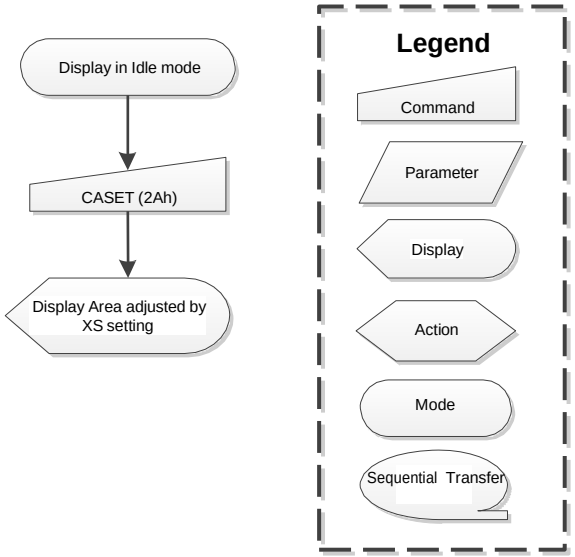
1. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, PIXEL_SHIFT_Y_COUNT, XS_ANC_SHT, and YS_ANC_SHT.
2. When anchor shift function is enable(EN_ANC=1), YS has no constraint.
3. Wen anchor shift function is disable(EN_ANC=0), YS has constraints as below:

a) PIXEL_SHIFT_Y_DIR=0(Up)
Parameter range= 0 ⩽ YS[15:0]*2 + NL[8:0]*4 - PIXEL_SHIFT_Y_COUNT*2 ⩽ 1104

b) PIXEL_SHIFT_Y_DIR=1(Down)
Parameter range= 0 ⩽ YS[15:0]*2 + NL[8:0]*4 + PIXEL_SHIFT_Y_COUNT*2 ⩽ 1104

Default

Status	Default Value	
Power On Sequence	2B00h	00h
	2B01h	00h
SW Reset	The same as above	
HW Reset	The same as above	



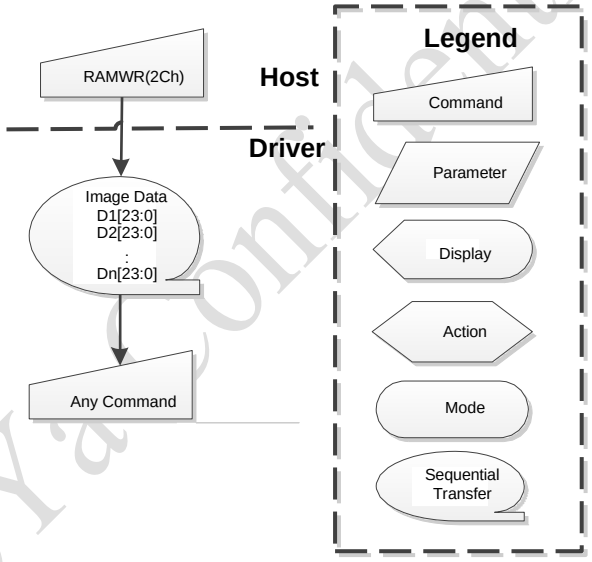
RAMWR(2C00h):Memory Write

2C00H	RAMWR											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RAMWR	W	2Ch	2C00h	-	D7	D6	D5	D4	D3	D2	D1	D0
			2C01h	-	D7	D6	D5	D4	D3	D2	D1	D0
			2C02h	-	D7	D6	D5	D4	D3	D2	D1	D0
Description	1.This command writes display data from the host to display driver's memory buffer. 2.When this command is accepted, the address of memory buffer is reset to its start position and the sequential data are write to memory byte to byte until a full frame display data.											
Restriction	Sending any command can stop writing frame memory.											

Default

Status	Default Value	
Power On Sequence	2C00h	00h
	2C01h	00h
	2C02h	00h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart

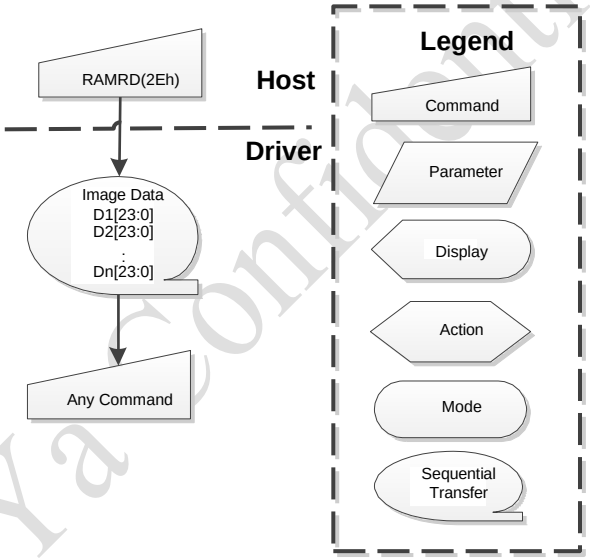


REMRD(2E00h):Memory Read

2E00H	RAMRD											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RAMRD	R	2Eh	2E00h	-	D7	D6	D5	D4	D3	D2	D1	D0
			2E01h	-	D7	D6	D5	D4	D3	D2	D1	D0
			2E02h	-	D7	D6	D5	D4	D3	D2	D1	D0
Description	1.This command reads display data from display driver's memory buffer to the host. 2.When this command is accepted, the address of memory buffer is reset to its start position and the sequential data are read to host byte to byte until a full frame display data.											
Restriction	Sending any command can stop frame memory read.											

Default	Status	Default Value	
	Power On Sequence	2E00h	00h
		2E01h	00h
		2E02h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



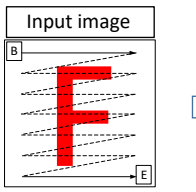
MADCTL (3600h): Set Address Mode

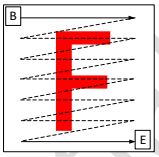
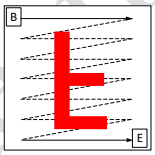
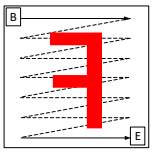
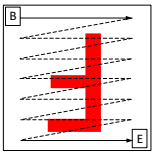
3600H	MADCTL										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	R/W	36h	3600h	-	-	-	-	-	D3	-	D1	D0

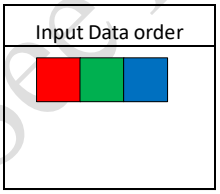
Description

This command set scan direction of source and gate and data order.

Bit	Symbol	Description	Comment
D3]	RGB	Color Order of sub-pixel of true RGB type	1=BGR 0=RGB
D1	RSMX	Horizontal Flip	1=Normal Display 0= Horizontal Flip
D0	RSMY	Vertical Flip	1= Normal Display 0= Vertical Flip



RSMX	RSMY	Display
0	0	
0	1	
1	0	
1	1	

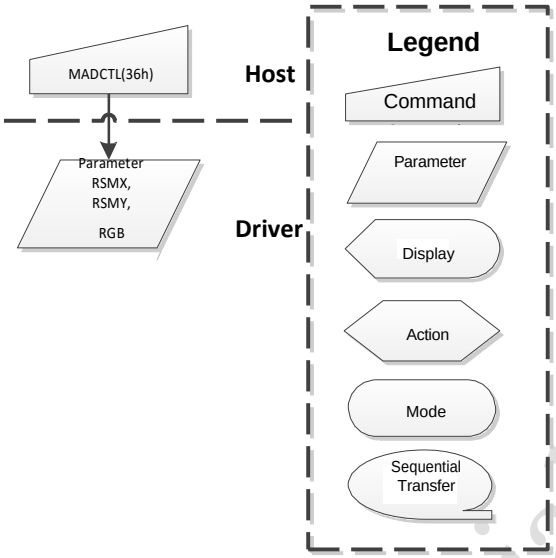


RGB	Panel Display Color Order
0	
1	

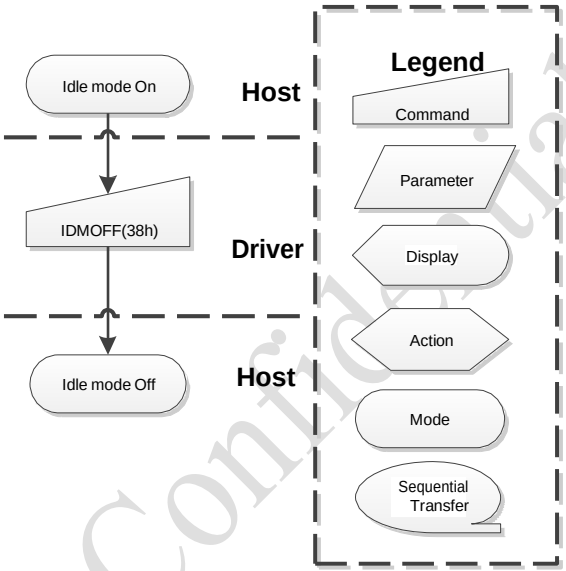
Restriction: -

Default

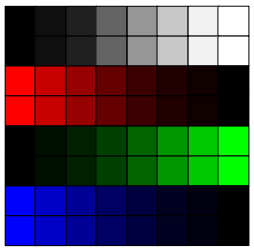
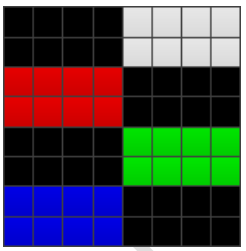
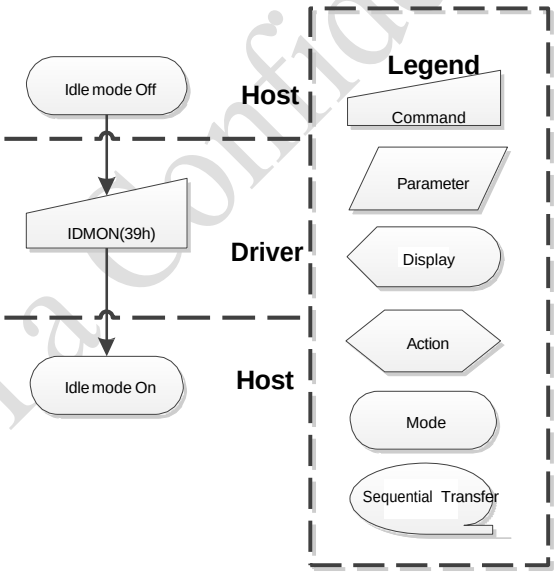
Status	Default Value	
Power On Sequence	3600h	00h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart	

IDMOFF (3800h): Idle Mode Off

3800H	IDMOFF											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	W	38h	3800h	-	No Parameter							
Description	This command cause display module to exit *Idle* mode.											
Restriction	This command has no effect when display module is not in *Idle* mode.											
Default	Status	Default Value										
	Power On Sequence	3800h	Idle mode off									
	SW Reset	The same as above										
	HW Reset	The same as above										
Flow Chart												

IDMON (3900h): Idle Mode On

3900H	IDMON										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
IDMON	W	39h	3900h	-	No Parameter							
Description	This command cause display module to enter *Idle* mode. In the *idle* mode, color expression is reduced. Input Image  Display 										
Restriction	This command has no effect when display module is already in *Idle* mode.										
Default	Status	Default Value									
	Power On Sequence	3900h	Idle mode on								
	SW Reset	The same as above									
	HW Reset	The same as above									
Flow Chart											

COLMOD (3A00h): Interface Pixel Format

3A00H	COLMOD										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
COLMOD	R/W	3Ah	3A00h	-	D[7:4]				IFPF[3:0]			

Description

This command indicates the current pixel format of the display:

Bit	Symbol	Description	Comment
D[7:4]	VIPF[3:0]	DPI Pixel Format	7=24-bit/pixel Others=Reserved
D[3:0]	IFPF[3:0]	DBI Pixel Format	7=24-bit/pixel Others=Reserved

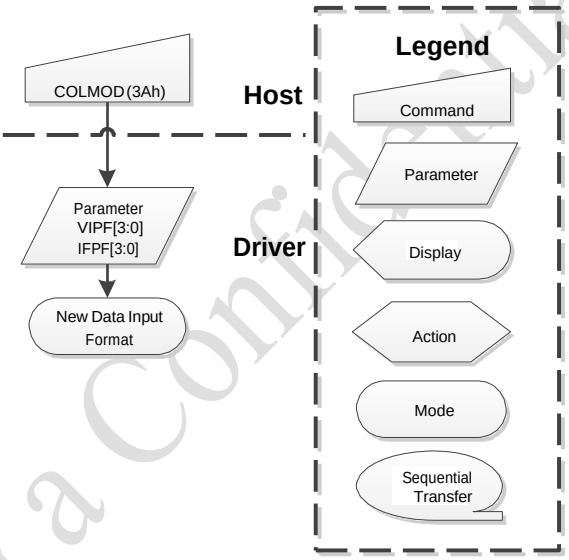
Restriction

-

Default

Status	Default Value	
Power On Sequence	3A00h	77h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart

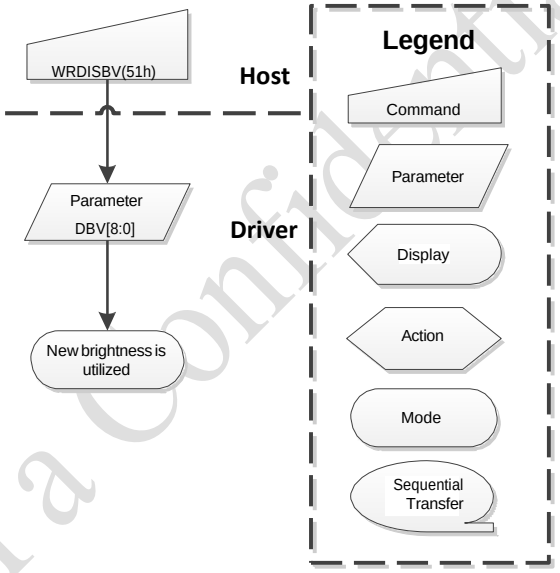


WRDISBV (5100h): Write Display Brightness

5100H	WRDISBV											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	W	51h	5100h	-	DBV[7:0]							
			5101h	-	-	-	-	-	-	-	-	DBV [8]
Description	This command is used to adjust brightness.											
Restriction	-											

Default	Status	Default Value	
	Power On Sequence	5100h	00h
		5101h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



SCACTRL (6900h): Scaling Up Control

6900H	SCACTRL										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
SCACTRL	R/W	69h	6900h	-	-	-	-	-	-	-	D[1:0]	

Description

This command sets operation mode of MIPI clock lane during porch time.

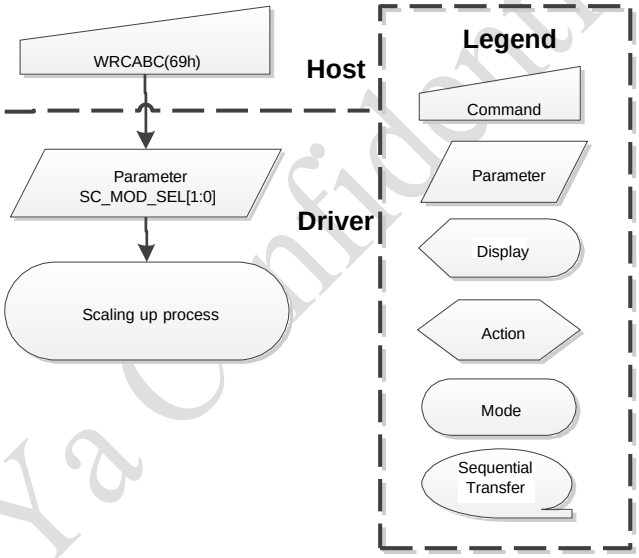
Bit	Symbol	Description	Comment
D[1:0]	SC_MOD_SEL	Scaling up ratio selection	0= off 1= 1.33x scaling up 2=1.5x scaling up 3= 2x scaling up

Restriction: -

Default

Status	Default Value	
Power On Sequence	6900h	00h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart



IFCONF (6B00h): Interface Configure

6900H	IFCONFG										
Instruction	R/W	Address		Parameter							
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
IFCONFG	R/W	6Bh	6B00h	-	-	-	-	-	-	-	D[1:0]	

Description

lane_num_cfg_CMD1: Set MIPI Lane selection. XOR with lane_num_cfg (CMD2 page0 B100).

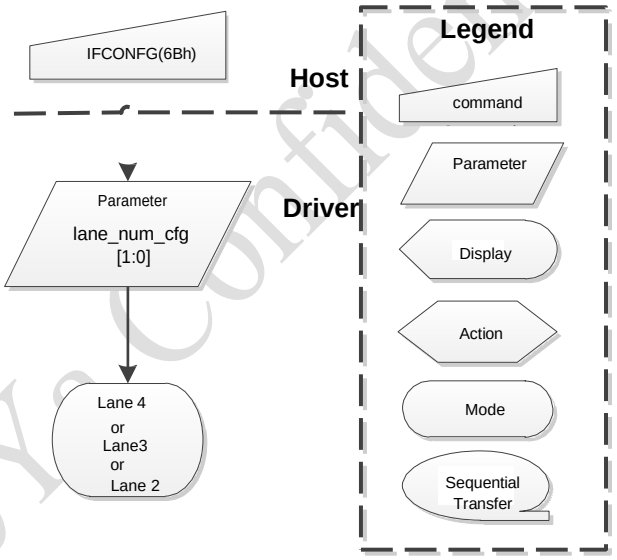
Bit	Symbol	Description	Comment
D[1:0]	lane_num_cfg_CMD1[1:0]	MIPI lane number selection	0:4-Lanes 1:3-Lanes 2:2-:Lanes 3:Reserved

Restriction: -

Default

Status	Default Value	
Power On Sequence	6B00h	10h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart

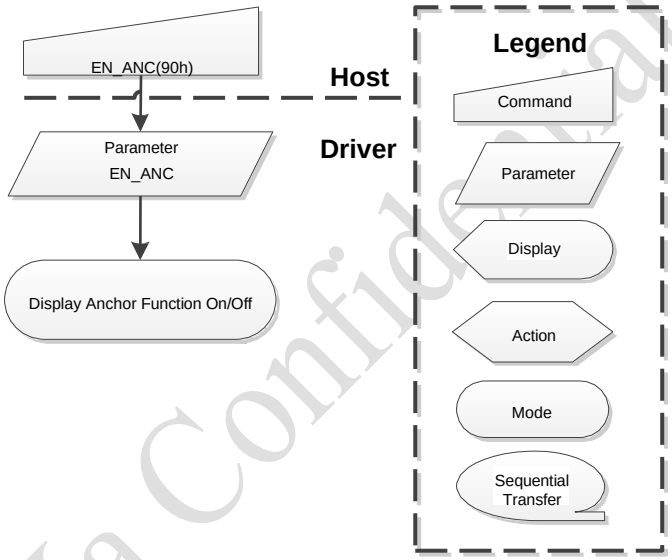


ANCTRL1 (9000h): Display Anchor On/Off

9000H	ANCTRL1											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
ANCTRL1	R/W	90h	9000h	-	-	-	-	-	-	-	-	EN_ANC
Description	This command is used to enable display anchor function. *Note*: Display anchor coordinate will be reset when display anchor function turn-off.											
Restriction	-											

Default	Status	Default Value	
	Power On Sequence	9000h	00h
	SW Reset	The same as above	
	HW Reset	The same as above	

Flow Chart



ANCTRL2 (9100h): Display Anchor CTRL

9100H	ANCTRL2											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
ANCTRL2	R/W	91h	9100h	-	-	-	-	XS_ANC_SHT_DIR	-	XS_ANC_SHT[10:8]		
	R/W		9101h	-	XS_ANC_SHT[7:0]							
	R/W		9102h	-	-	-	-	YS_ANC_SHT_DIR	-	YS_ANC_SHT[10:8]		
	R/W		9103h	-	YS_ANC_SHT[7:0]							

Description

This command is used to adjust display anchor.

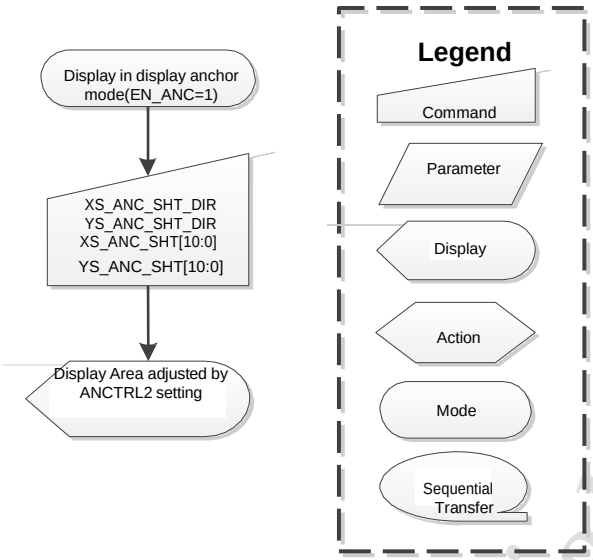
Bit	Symbol	Description	Comment
D[4]	XS_ANC_SHT_DIR	Display anchor shift direction of X-axis	1:Right 0:Left
D[4]	YS_ANC_SHT_DIR	Display anchor shift direction of Y-axis	1:Down 0:Up
D[7:0]	XS_ANC_SHT[10:0]	Display anchor shift steps of X-axis	XS_ANC_SHT[10:0] / Anchor shift steps of X-axis 0 / 0-step 1h / 1-step 2h / 2-step : / : 3FDh / 1021-step 3FEh / 1022-step 3FFh / 1023-step
D[7:0]	YS_ANC_SHT[10:0]	Display anchor shift steps of Y-axis	YS_ANC_SHT[10:0] / Anchor shift steps of Y-axis 0 / 0-step 1h / 1-step 2h / 2-step : / : 3FDh / 1021-step 3FEh / 1022-step 3FFh / 1023-step

Note: Display anchor shift distance for X-axis and Y-axis is described as below:
Anchor shift step of X-axis=8.4um
Anchor shift step of Y-axis=11.2um

Restriction: The display anchor shift settings are valid when display anchor function is enabled(EN_ANC=1).

Default

Status	Default Value	
Power On Sequence	9100h	00h
	9101h	00h
	9102h	00h
	9103h	00h
SW Reset	The same as above	
HW Reset	The same as above	

Flow Chart	

12 Reliability

No.	Item	Condition	Judgement Criterion
1	High Temperature Storage	80℃ 240hrs	After testing 1.No clearly visible defects or remarkable deterioration of display quality. 2.No function-related abnormalities *The results must be checked after 2hours later under room temperature
2	High Temperature Operating	70℃ 240hrs	
3	Low Temperature Storage	-40℃ 240hrs	
4	Low Temperature Operating	-20℃ 240hrs	
5	High Temperature / Humidity Storage	60℃/90%RH 240hrs	
6	High Temperature / Humidity Operating	60℃/90%RH 240hrs	
7	Thermal Shock	-30℃ ←→ 80℃, 0.5hr, Change time <1min, 100cycles	
8	ESD	Air discharge ±2kv Contact discharge ±1kv	After testing 1.Hard defect should not happen 2.If it would be recovered to normal state after resetting, it would be judged as a good state.

13 Handling Precautions

13.1 Mounting Method

This Micro-OLED product consists of one silicon backplane and one cover glass, which can easily get damaged. Extreme care should be used when handling the MICRO-OLED.

13.2 Caution of Against Static Charge

For this Micro-OLED, use C-MOS drivers, do not input and signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects Micro-OLED. Against static charge, you should make sure that the product is safe or not by experiment in advance.

13.3 Packing

The packing principle is that Micro-OLED module should keep its packing condition at the time of delivery. For safety & avoiding the module damage, Carton box must stack the below 4 boxes.

When storing the Micro-OLED after unpacking, note the followings. Micro-OLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.

To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

13.4 Caution for Operation

If you do not follow normal POWER ON, OFF sequence or abnormal operating, then Micro-OLED module can be damaged electro-optically and does not recover. Do not change software without SeeYA confirmation.

Micro-OLED module may not display normally when twisting power or pressing power is added. Therefore, you should secure Micro-OLED module maximum thickness at set assembly not to have any pressure affect Micro-OLED module.

Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use MICRO-OLED Module below maximum operating humidity.

Micro-OLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage Micro-OLED module by surrounding elements.

To satisfy EMI standards, you should plan your design after considering emitting energy. We can't guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area. Image-sticking may occur if Micro-OLED displays same image for a long time, so you need to make a change for Micro-OLED.

13.5 Storage

Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity. Store with no contact with polarizer surface. It is recommended to store them as they have been contained in the inner container when we delivered them.

13.6 Safety Precautions

Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMICRO-OLED module, dust adhesion, or scratches on the display part. In the event that the contents of AMICRO-OLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary. Do not use the AMICRO-OLED module for the special purpose besides display units. Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken. For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

13.7 Precautions before use

You should discuss the following case with SeeYA:

- in case of any questions about contents of this "Specification for Approval".
- in case of occurring new problems not mentioned at this "Specification for Approval".
- in case of your request about income inspection specification change.
- in case of occurring new problem at your driving test.

*If SeeYA has to change the conditions specified in the specification, previously shall be held and decided.

14 Warranty

Basically, warranty term is 12 months of reliability characteristics of quality level after the outgoing date in SeeYA, could compensate for defectives which happens within warranty term under condition that the products should be stored or be used as specified under normal condition within the contents of specification.

Otherwise, it is impossible to compensate for defectives when they happen by customer's mistake such as careless handing or circuit change, etc.

15 Packing