FORMIKE® GROUP
LCD·SOLUTION·TOUCHSCREEN

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH101KQ14-C01 Version: 1.0

【 】 Preliminary Specification
【 ◆ 】 Finally Specification

CUSTOMER'S APPROVAL Chunho Tech	
SIGNATURE:	DATE:

●It signifies that you fully understand and accept all the contents of this specification if you sign and send back the first page of this specifications.

Designed by	R&D Checked by	Quality Department by	Approved by
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Revision record

REV NO.	REV DATE	CONTENTS	Note
V1.0	**2019-09-09**	**NEW ISSUE**	LEO

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1. General Description

1.1 Description

KWH101KQ14-C01 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC,CTP and backlight unit . The following table described the features of FORMIKE KWH101KQ14-C01.

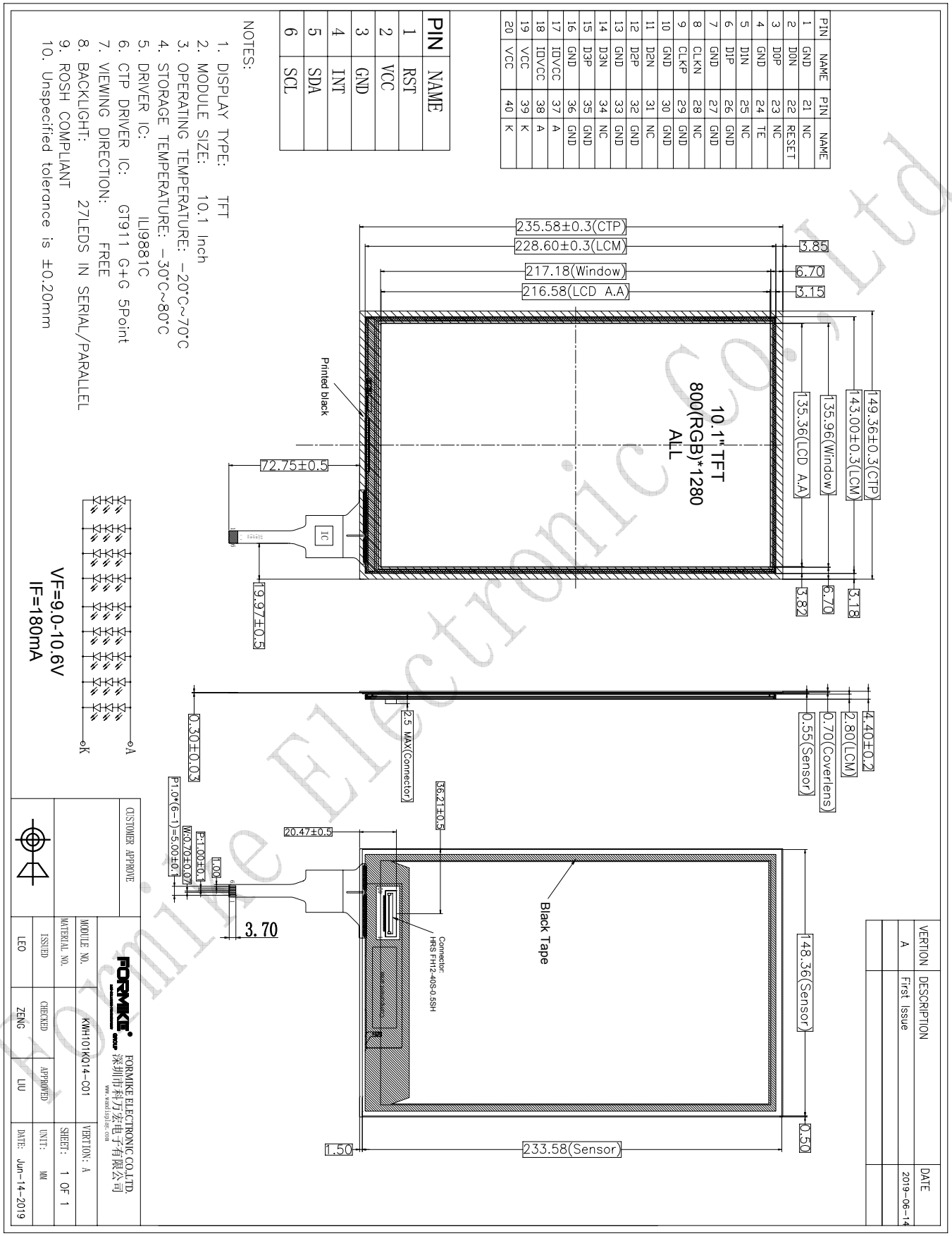
1.2 Application

Mobile phone, Multimedia products
and other electronic Products
Etc.

1.3 Features:

Features	Description	UNITS
LCD type	10.1”TFT	--
Dot arrangement	800（RGB）×1280	dots
Driver IC	ILI9881C	--
Color Depth	16M	
Interface	4 LANES MIPI	
Module size	149.36 (W) ×235.58 (H)×4.40 (T)	mm
Active area	135.36(W) ×216.58(H)	mm
Dot pitch	0.1692(W) ×0.1692(H)	mm
Back Light	27 White LED	--
With/Without TSP	With TSP	
Weight(g)	TBD	

2. External Dimensions



3. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground.
2	MIPI_0N	MIPI DSI differential data pair. (Data lane 0)
3	MIPI_0P	MIPI DSI differential data pair. (Data lane 0)
4	GND	Ground.
5	MIPI_1N	MIPI DSI differential data pair. (Data lane 1)
6	MIPI_1P	MIPI DSI differential data pair. (Data lane 1)
7	GND	Ground.
8	MIPI_CKN	MIPI DSI differential clock pair
9	MIPI_CKP	MIPI DSI differential clock pair
10	GND	Ground.
11	MIPI_2N	MIPI DSI differential data pair. (Data lane 2)
12	MIPI_2P	MIPI DSI differential data pair. (Data lane 2)
13	GND	Ground.
14	MIPI_3N	MIPI DSI differential data pair. (Data lane 3)
15	MIPI_3P	MIPI DSI differential data pair. (Data lane 3)
16	GND	Ground.
17	IOVCC	Power supply for internal logic regulator.
18	IOVCC	Power supply for internal logic regulator.
19	VCC	Power supply for analog circuits.
20	VCC	Power supply for analog circuits.
21	NC	No connection.
22	RESET	System reset pin
23	NC	No connection.
24	TE	Tearing effect output pin.Leave it open when not in use.
25	NC	No connection.
26	GND	Ground.
27	GND	Ground.
28	NC	No connection.
29	GND	Ground.
30	GND	Ground.
31	NC	No connection.
32	GND	Ground.
33	GND	Ground.
34	NC	No connection.
35	GND	Ground.
36	GND	Ground.
37	A	Anode input for backlight
38	A	Anode input for backlight
39	K	Cathode input for backlight
40	K	Cathode input for backlight

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	**V_{CC}**	**-0.3**	**4.6**	**V**
Supply voltage for logic	**V_{CCIO}**	**-0.3**	**4.6**	**V**
Operating temperature	**T_{OP}**	**-20**	**+70**	**°C**
Storage temperature	**T_{ST}**	**-30**	**+80**	**°C**

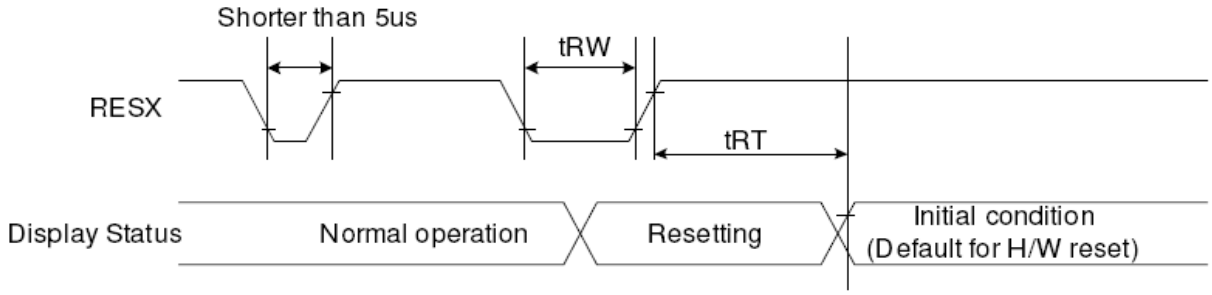
*The absolute maximum rating is listed on above table.
*When the LCM is used out of the absolute maximum ratings, it may be permanently damaged.
*To use the LCM within the above electrical characteristics limitation is strongly recommended for normal operation.
*If these electrical characteristic conditions are exceeded during normal operation, LCM will malfunction and cause poor reliability.

5. Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Applicable terminal
Supply voltage	**V_{CC}**	**2.4**	**2.8**	**3.3**	**V**	**V_{CC}**
Supply voltage for logic	**V_{CCIO}**	**1.65**	**1.8**	**3.3**	**V**	**V_{CCIO}**
Input voltage	**V_{IL}**	**0**	**-**	**0.3V_{CC}**	**V**	
	V_{IH}	**0.7 V_{CC}**	**-**	**V_{CC}**	**V**	

6.Timing Characteristics.

6.1 Reset Timing Characteristics.



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

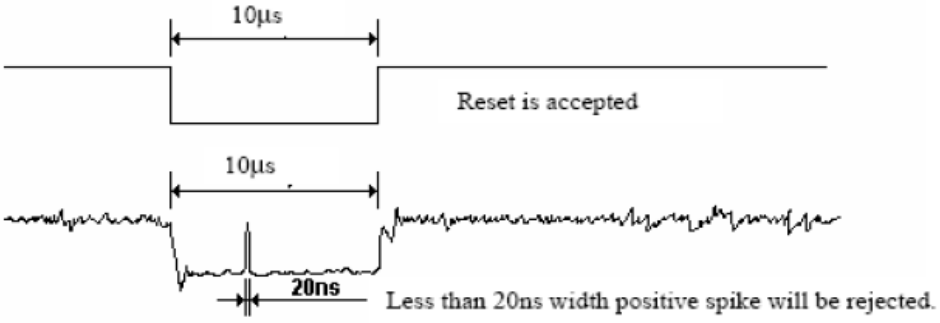
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6.2 Interface Timing Characteristics.

6.2.1 High Speed Mode-Clock Channel Timing.

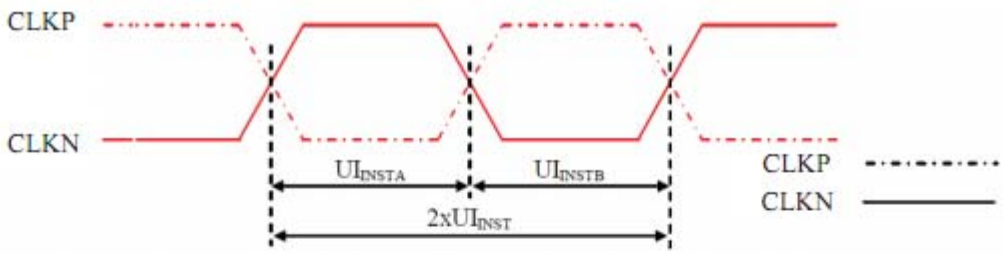


Figure: DSI Clock Channel Timing

Table: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table.

Table: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

6.2.2 High Speed Mode-Data Clock Channel Timing .

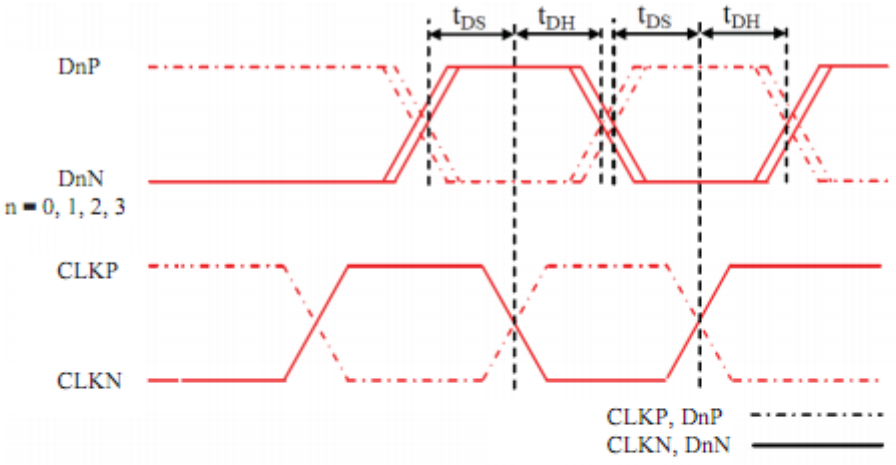


Figure: DSI Data to Clock Channel Timings

Table: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6.2.2 High Speed Mode-Rising and Falling Timings .

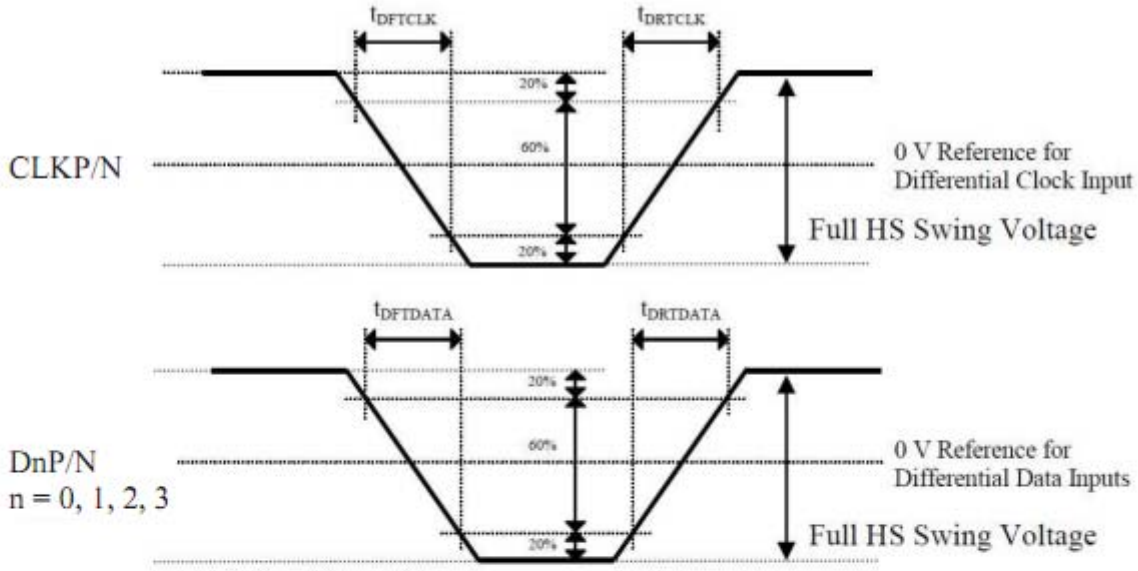


Figure: Rising and Falling Timings on Clock and Data Channels

Table: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

6.2.3 Low Speed Mode-Bus Turn Around.

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881) are illustrated for reference purposes below.

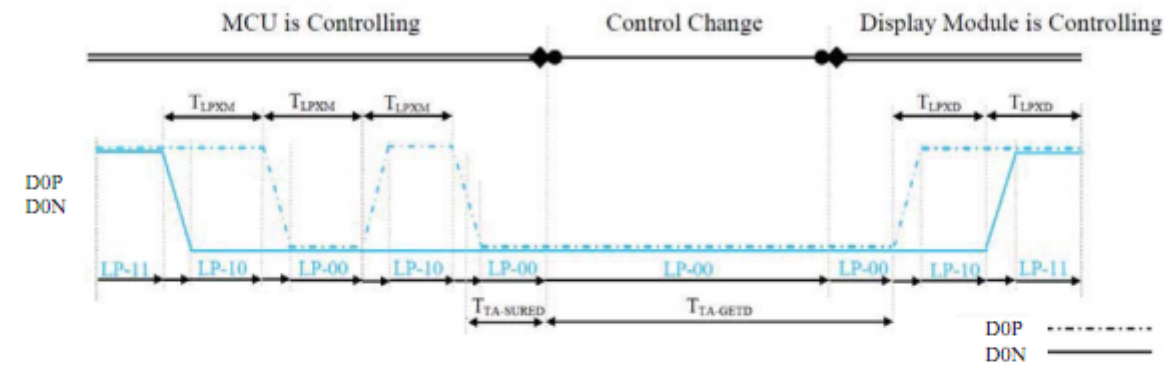


Figure: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881) to the MCU are illustrated for reference purposes below.

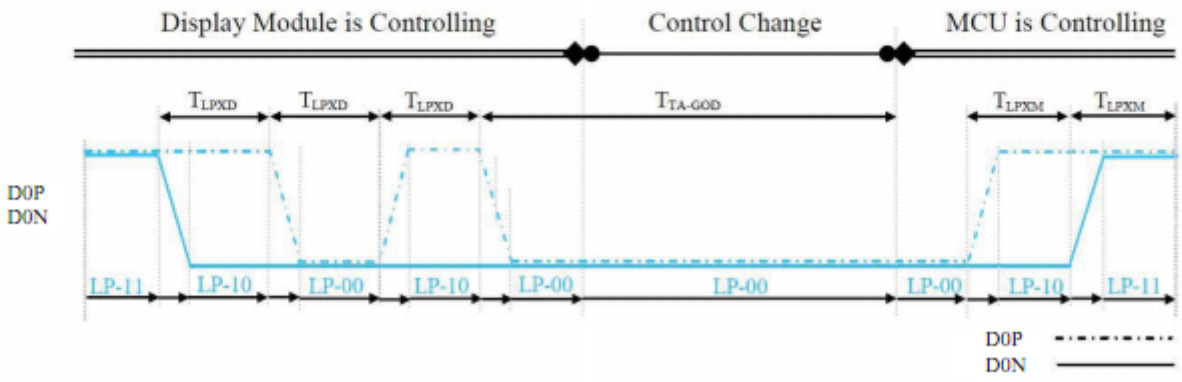


Figure: BTA from the Display Module to the MCU

Table: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

6.2.4 Data Lanes from Low Power Mode to High Speed Mode.

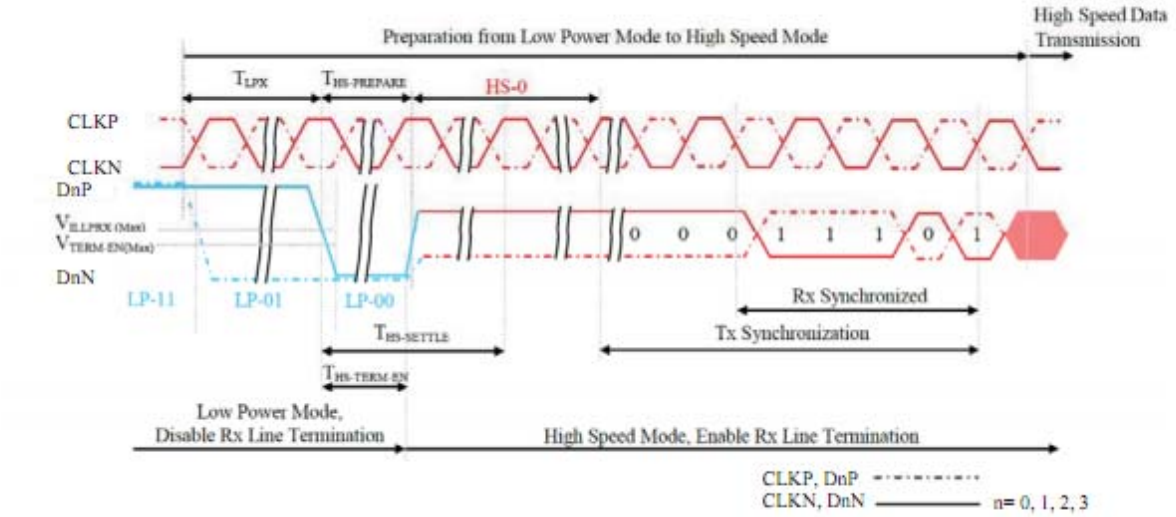
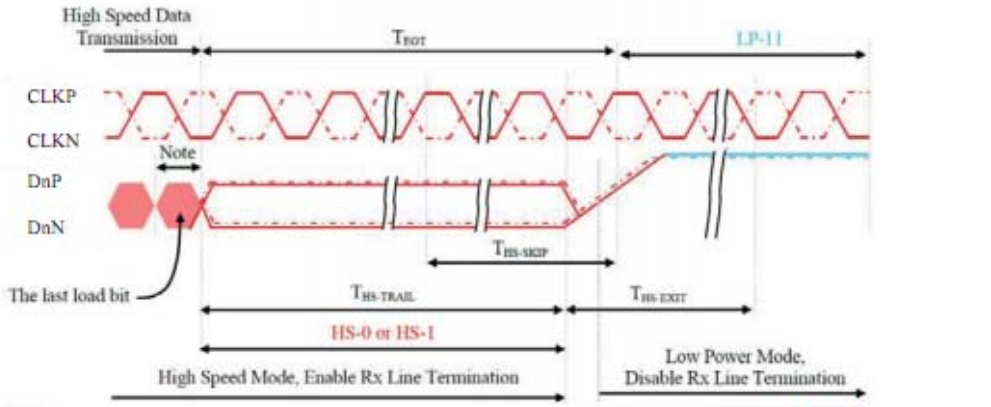


Figure: Data Lanes - Low Power Mode to High Speed Mode Timings

Table: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

6.2.5 Data Lanes from High Speed Mode to Low Power Mode.



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 123: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

6.2.6 DSI Clock Burst-High Speed Mode to/from Low Power Mode .

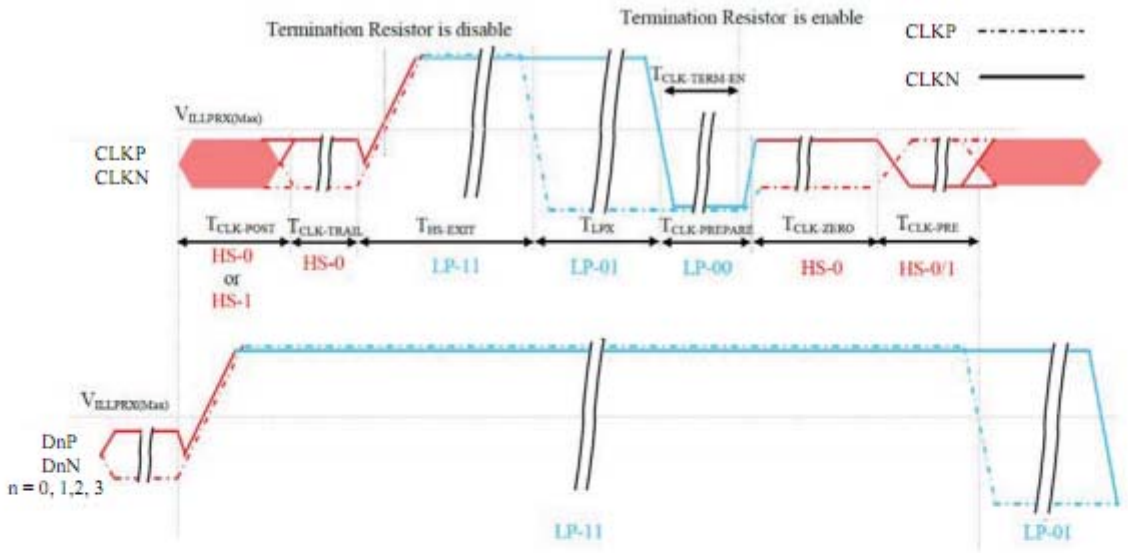
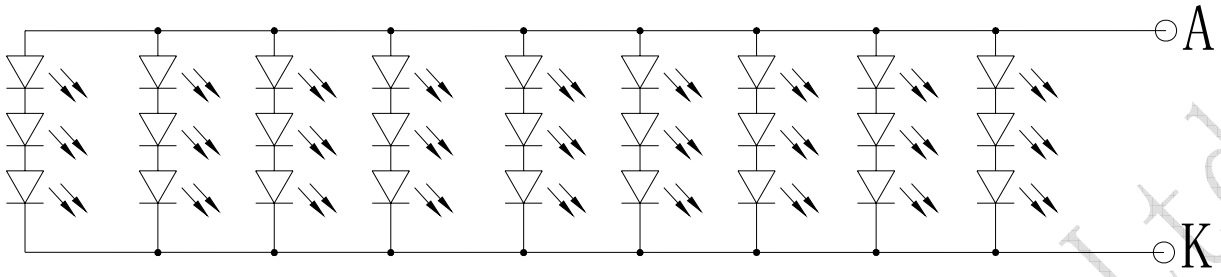


Figure 124: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

7. Backlight Characteristics.



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	**Vf**	**9.0**	**9.6**	**10.6**	**V**	**If=180 mA**	**-**
Supply Current	**If**	**-**	**180**	**-**	**mA**	**-**	**-**
Reverse Voltage	**Vr**	**-**	**-**	**5**	**V**	**10uA**	
Power dissipation	**Pd**	**-**	**1728**	**-**	**mW**	**-**	
Luminous Intensity for LCM		**200**	**220**	**-**	**Cd/m2**	**If=180 mA**	
Uniformity for LCM	**-**	**75**	**80**	**-**	%	**If=180 mA**	
Life Time	**-**	**50000**	**-**	**-**	**Hr**	**If=180 mA**	**-**
Backlight Color	**White**						

8. Touch panel Characteristics.

8.1 Interface Description:

PIN NO.	PIN NAME	DESCRIPTION
1	RST	Reset for system
2	VCC	Power supply voltage
3	GND	Ground
4	INT	Interrupt output for CTP.
5	SDA	Data signal for IIC interface.
6	SCL	Clock signal for IIC interface.

8.2 Features :

Item	Description
Interface	IIC
Touch Linearity	3%
Surface hardness	≥6H
Transmittance	≥85%
Structure type	G+G(Glass+Glass)
Lifetime	≥1,000,000 times
Driver IC	GT911
Touch points	5 points

8.3 Electronic Characteristics :

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	VCC	2.8	3.3	3.6	V		-
Input high-level voltage	VIH	0.7*VCC	-	VCC	V		
Input low -level voltage	VIL	-0.3		0.3*VCC	V		
Output high -level voltage	VOH	0.7*VCC	-	-	V		
Output low -level voltage	VOL	-	-	0.3*VCC	V		

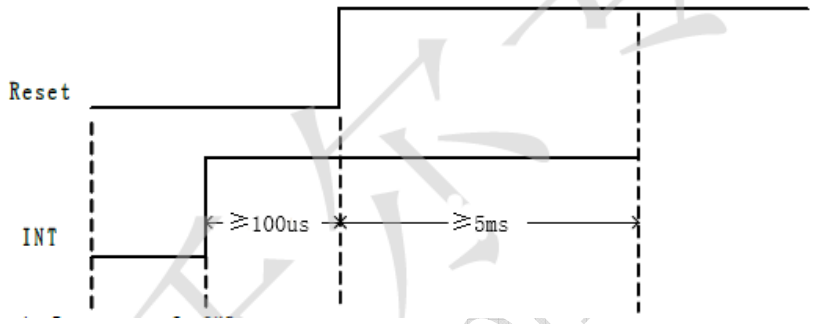
8.4 IIC Interface Timing.

VCC=3.3V,pull up resistance 2K.

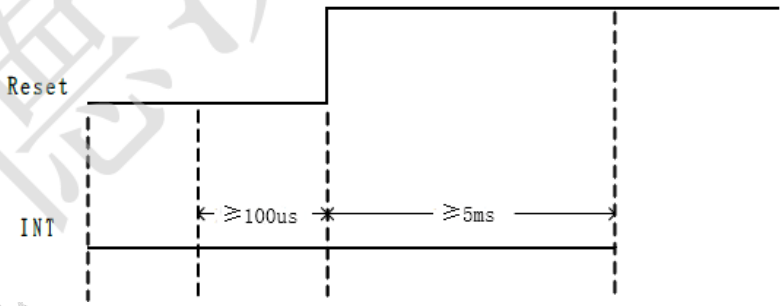
Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	Us

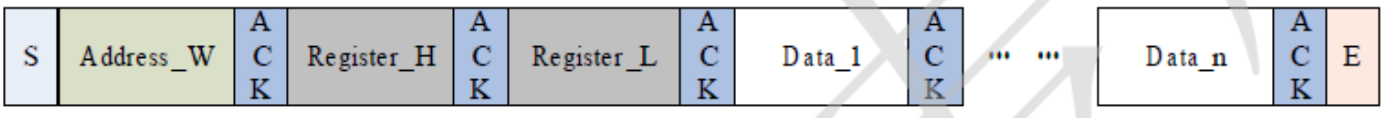
I2C Address 0x28/0x29 setting



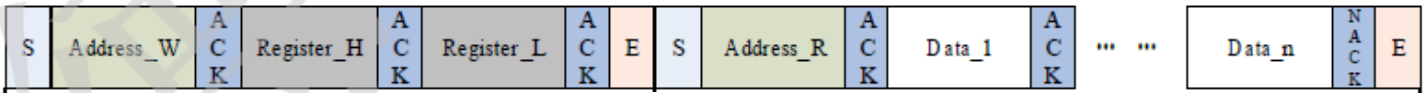
I2C Address 0xAB/0xBB setting



I2C Serial Data Transfer Format



I2C master write, slave read



I2C master read, slave write

9.Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	Θ=0 Normal viewing angle	—	5.7	—	%	Measuring with Polarizer，Reference Only
Transmittance (without Polarizer)		T (%)		—	TBD	—	%	
Contrast		CR		TBD	800	—	—	(1)(2)
Response time	Rising	T_R		—	10	15	msec	(1)(3)
	Falling	T_F		—	20	25		
Color gamut	(%)			45	60	—	%	C-light
Color chromaticity (CIE1931)	White	W_x		0.28	0.31	0.34	—	(1)(4) CF glass
		W_y		0.30	0.33	0.36		
	Red	R_x		TBD	TBD	TBD	—	
		R_Y		TBD	TBD	TBD	—	
	Green	G_x		TBD	TBD	TBD	—	
		G_Y		TBD	TBD	TBD		
	Blue	B_x		TBD	TBD	TBD	—	
		B_Y		TBD	TBD	TBD		
Viewing angle	Hor.	Θ_L	CR>10	—	89	—	—	(1)(4) Measuring with Polarizer，Reference Only
		Θ_R		—	89	—		
	Ver.	Θ_U		—	89	—		
		Θ_D		—	89	—		
Optima View Direction		ALL						(5)

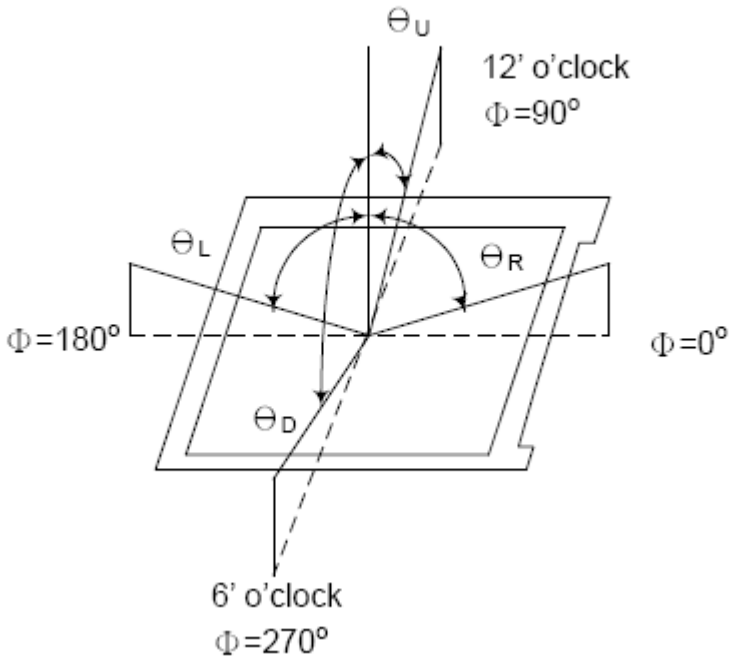
Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

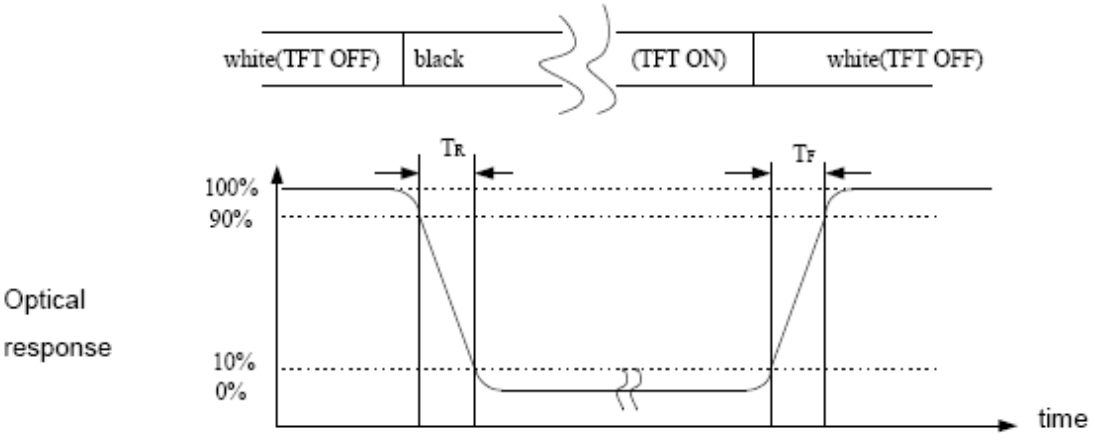
Note (1) Definition of Viewing Angle :



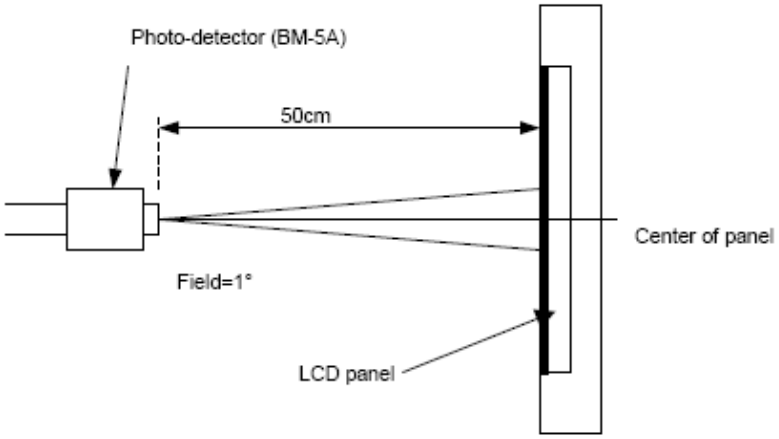
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

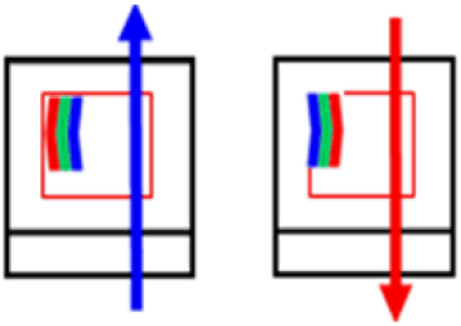
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



Array Film Up

CF Film Up

10. RELIABILITY

No.	Test Item	Test Condition	Remark
1	High Temperature Storage	+80℃± 2℃，96 hrs	Note
2	Low Temperature Storage	-30℃± 2℃，96 hrs	Note
3	High Temperature Operation	+70℃± 2℃，96 hrs	Note
4	Low Temperature Operation	+20℃± 2℃，96 hrs	Note
5	High Temperature & High Humidity Storage Test	+50℃± 5℃, 90％R.H, 96 hours	Note
6	Temperature Cycle (non operation)	-30℃ ← +25℃ → +80℃ (30mins ← 5mins →30mins) 10 Cycles	Note
7	Electronic Static Discharge	Air Discharge: 2KV to with 5 times Ambiance: 15℃~35℃,30%~60%R.H Resistance(Rd): 330Ω ±10% Capacitance(Cs + Cd): 150pF±10%	Discharge for each polarity Mode of Operation: Single Discharge, successive discharge at least 1 sec
8	Vibration (Packaged)	Frequency range: 10Hz ~ 55 Hz Amplitude: 1.5mm Direction of X.Y. Z for 3 Hrs in total	
9	Drop Test (Packaged)	Height: 80cm, Time: 1 1 corner, 3 edged, 6 surfaces	

Note : Recovery Time should be 2~4 hours at room temperature (20±8℃) and humidity (below 60% R.H). No abnormalities in functions and appearance

11.INSPECTION CRITERION

11.1 Scope

Display Quality Evaluation
Mechanics Specification

11.2 Sampling Plan

MIL-STD-105E
Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD-105E
Lot size: Quantity per shipment as one lot (different model as different lot).
Sampling type: Normal inspection, single sampling
Sampling level: Level II.

11.3 Acceptable Quality Level

Item	Major	Minor
Appearance	1.0%	1.5%
Electrical	0.65	1.0%

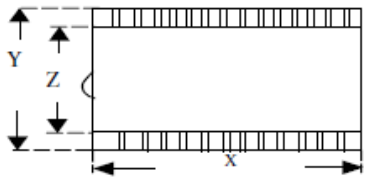
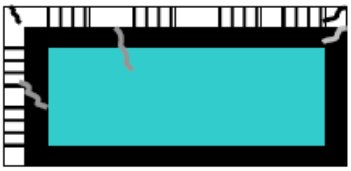
11.3.1 Classification of defects：
11.3.1.1Major defect
Any defect may result in functional failure, or reduce the usability of product for its purpose. For Example：Electrical failure, deformation and etc.
11.3.1.2 Minor defect
The criteria on major or minor judgment will be according with the classification of defects.

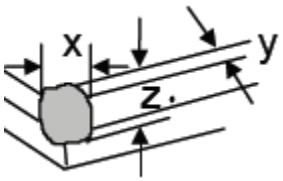
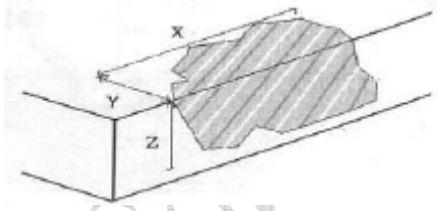
11.4 Panel Inspection Condition

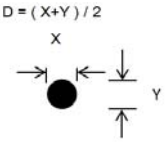
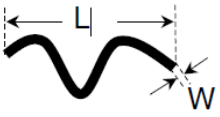
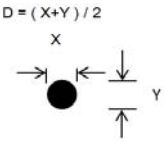
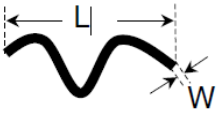
11.4.1 Environment:
11.4.2 Room Temperature: 25±5° C.
11.4.3 Humidity: 50±20% RH.
Illumination: 300 ~ 700 Lux.
11.4.4 Inspection Distance: 35±5 cm

11.5 TFT Inspection Criteria

11.5.1 Visual inspection criterion in cosmetic / appearance

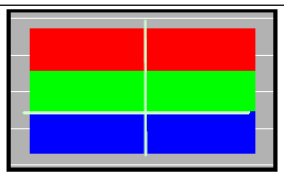
Glass defect			
No	Item	Criteria	Remark
1	Dimension (Minor)	By engineering diagram	
2	Crack (Major)	Extensive crack	

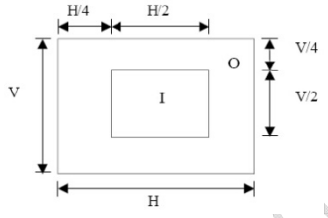
3	Corner (Minor)	X ≤3 mm Y ≤3 mm Z≤ T Ignore	 T: Glass thickness Z: Thickness X: Length Y: Width
4	Side (Minor)	X ≤5mm Y ≤3 mm Z≤ T Ignore	 T: Glass thickness Z: Thickness X: Length Y: Width

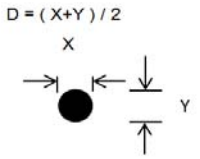
TFT defect in appearance			
No	Item	Criteria	Remark
1	Foreign Spot (Minor) Including: Black spot, White spot Pin hole Foreign particle	D≤0.25mm，Ignore 0.25mm<D≤0.5mm，N≤3 0.5mm<D，N=0 Distance≥5mm Ignore if out of Area AA	D =(X+Y)/2, X: Length, Y: Width 
2	Foreign Line(Minor) Including: Black line White line Bright line	W≤0.03mm，Ignore 0.05mm<W≤0.08mm, L≤4mm, N≤3 0.08mm<W≤0.10mm, L≤4mm, N≤1 W>0.10mm, N=0 Ignore if out of Area AA	L: Length, W: Width 
3	Polarizer Dent/Air Bubble (Minor)	D≤0.25mm，Ignore 0.25mm<D≤0.5mm，N≤4 D>0.50mm, N=0 Distance≥5mm	D =(X+Y)/2, X: Length, Y: Width 
4	Polarizer Scratches (Minor)	W≤0.05mm，Ignore 0.05mm<W≤0.08mm, L≤4mm, N≤3 0.08mm<W≤0.10mm, L≤4mm, N≤1 W>0.10mm, N=0 Ignore if out of Area AA	L: Length, W: Width 

Other defects			
No	Item	Criteria	Remark
1	FPC (Minor)	Any crack or breakage which effect the function are not allowed Disregard if the dirty removed	
2	Backlight (Minor)	Power up is allowed. Breaking off is not allowed. The scratch which may causes a problem in practical use is not allowed	
3	Bezel (Minor)	Erasable dirt is ignore	

11.5.2 Visual inspection criterion in electrical display

Glass defect			
No	Item	Criteria	Remark
1	No display (Major) Abnormally Short circuit	Not allowed	
2	Missing line (Major)	Not allowed	
3	Darker or lighter line (Major)	Not allowed	
4	Weak line (Minor)	By limit sample	

<table>
<tr><td colspan="4">Display Inspection</td></tr>
<tr><td>No</td><td>Item</td><td>Criteria</td><td>Remark</td></tr>
<tr><td>1</td><td>Bright / Dark dot</td><td>
<table>
<tr><td>Items</td><td>Area I</td><td>Area O</td><td>Total</td></tr>
<tr><td>Bright</td><td>1</td><td>2</td><td>2</td></tr>
<tr><td>Dark</td><td>2</td><td>3</td><td>4</td></tr>
<tr><td>Bright & Dark</td><td>2</td><td>4</td><td>5</td></tr>
<tr><td>2 adjacent dots</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">Minimum Distance ≥ 5mm</td></tr>
</table>
</td><td> 

1.1sub-pixel: 1R or 1G or 1B
2.Point defect area≥ 1/2 sub pixel</td></tr>
<tr><td>2</td><td>Tiny bright dot</td><td>Visible through 6% ND filter
D≤0.25mm，Ignore
0.25mm<D≤0.5mm，N≤4
D>0.5mm, N=0
Distance≥5mm
Ignore if out of Area AA</td><td>D =(X+Y)/2,
X: Length, Y: Width
 
</td></tr>
<tr><td>4</td><td>Mura/Waving/ Hot spot</td><td>Not visible through 6% ND filter in 50% gray or judge by limit sample if necessary</td><td></td></tr>
</table>

* Note:
1. Defect which is on the Black Matrix (outside of active area) are not considered as a defect.
2. If any specific defect is not included in the above defect table, this defect should be judged by Formike.
3. W：Width, L：Length D：Average Diameter N: Count.

12. PRECAUTION RELATING & PRODUCT HANDLING

Display is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification.

12.1 SAFETY

12.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.

12.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

12.2 HANDLING

12.2.1 Avoid any strong mechanical shock which can break the glass.

12.2.2 Avoid static electricity which can damage the CMOS LSI - When working with the module, be sure to ground your body and any electrical equipment you may be using. The followings should be noted:

12.2.2.1 CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.

12.2.2.2 Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.

12.2.2.3 Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.

12.2.2.4 The modules should be kept in anti-static bags or other containers resistant to static for storage.

12.2.2.5 Only properly grounded soldering irons should be used.

12.2.2.6 If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.

12.2.2.7 The normal static prevention measures should be observed for work clothes and working benches.

12.2.3.8 Since dry air is inductive to static, a relative humidity of 50-60% is recommended

12.2.3 Do not remove the panel or frame from the module.

12.2.4 The polarizing plate of the display is very fragile. Please handle it very carefully, do not touch, push or rub the exposed polarizing with anything harder than an HB pencil lead (glass, tweezers, etc.)

12.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

12.2.6 Do not touch the display area with bare hands, this will stain the display area.

12.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

12.2.8 To control temperature and time of soldering is 300± 10℃and 3-4 sec.

To avoid liquid (include organic solvent) stained on LCD Module.

12.3 STORAGE

12.3.1 Store the panel or module in a dark place where the temperature is 25℃±5℃and the humidity is below 60% RH.

12.3.2 Avoid exposure to direct sunlight or to the light of fluorescent lamps.

12.3.3 Do not place the module near organic solvents or corrosive gases.

Do not crush, shake, or jolt the module.

12.4 LIMITED WARRANTY

12.4.1 FORMIKE modules are not consumer products, but may be incorporated by FORMIKE's customers into consumer products or components thereof, FORMIKE does not warrant that its modules and components are fit for any such particular purpose.

12.4.2 The liability of FORMIKE is limited to repair or replacement on the terms set forth below. FORMIKE will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between FORMIKE and the customer, FORMIKE will only replace or repair any of its Modules which is found defective electrically or visually when inspected in accordance with FORMIKE INSPECTION CRITERIA

12.4.3 No warranty can be granted if any of the precautions state in handling liquid crystal display has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.

12.4.4 In returning the modules, they must be properly packaged; there should be detailed description of the failures or defect.

13. OTHERS

13.1 If there is any not specified quality standard in this specification as well as RMA , please refer to < INSPECTION CRITERIA>. Contact FORMIKE to get the complete <INSPECTION CRITERIA> by the contact window or feedback@wandisplay.com.

13.2 Special agreement of <INSPECTION CRITERIA> is recognized only in writhing between FORMIKE and the customer also indicated it before ordering.